# RTDS® SIMULATOR

## TECHNICAL DESCRIPTION

Table of Contents

# 1 INTRODUCTION

RTDS Technologies is pleased to provide the following technical description for the RTDS® Simulator.

The installation of an RTDS Simulator provides a state of the art, real time simulator for general power system studies, power electronic investigations, Hardware-In-the-Loop (HIL) testing of protective relay and control systems, Smart Grid and Distributed Energy Resources studies, Power-Hardware-In-the-Loop (PHIL) simulations, training, as well as research and development (note that additional equipment may be required depending on the application).

The RTDS Simulator is a modular, fully digital power system simulator that can be used for a wide range of studies. The final size and configuration of the simulator hardware is based on the topology and size of the network(s) to be studied as well as the purpose of the study and the external devices that it will be connected to. Appendix 1 of this proposal illustrates the general method of core allocation for the NovaCor-based simulator. Several simulation circuits are included in the Appendix along with core allocation tables. These examples are for illustrative purposes only.

# 2 RTDS SIMULATOR APPLICATIONS

The RTDS Simulator is widely applied in many areas, including:

- Control and Protection system testing
  - Line Commutated Converter (LCC)-based HVDC and UHVDC
  - MMC-based HVDC
  - 2- and 3-level converter-based HVDC
  - SVC (network and industrial)
  - FACTS (including STATCOM, UPFC, SSSC, DVR, etc.)
  - TCSC series compensation
  - Exciter and voltage regulators for synchronous machines
  - Governors for synchronous machines
  - Power System Stabilizers (PSS)
  - Distributed Generation and Renewables (wind, solar, fuel cell, etc.)
  - Smart Grid (IEC 61850, RAS – remedial action schemes, SCADA interface, etc.
- Protective Relay testing
  - Closed-loop testing of individual relays and relaying schemes
    - Line protection (impedance and differential)
    - Transformer protection
    - Generator protection
    - Busbar protection (low and high impedance schemes)
    - Etc.

- Conventional protection device testing using power amplifiers
- IEC 61850 compliant protection device testing
  - GOOSE messaging (subscribe and publish)
  - IEC 61850-9-2 (subscribe and publish)
  - IEC 61869-9 (publish)
- Remedial Action Schemes (RAS)
- Wide Area Monitoring, Protection, and Control (WAMPAC)

- Power electronics
  - HVDC – conventional and VSC based schemes
    - System design
    - Closed-loop control system design and verification testing
    - AC system impact studies
    - VSC-based schemes with 2- and 3-level converts as well as Modular Multi-level Converters (MMC)
  - FACTS – SVC, TCSC, STATCOM, UPFC, SSSC, etc.
    - System design
    - Closed-loop control system design and verification testing
    - AC system impact studies
    - VSC-based schemes with 2- and 3-level as well as MMC converters
  - Motor drives
    - Closed-loop control system design and verification testing
    - Configurable converter models and topologies
  - General Power Electronic Circuits
- Smart Grid and Renewables
  - Study and integration of renewables
    - Wind power with various configurations including Doubly Fed Induction Generator (DFIG) and Permanent Magnet Synchronous Machine (PMSM)
    - Solar
    - Fuel cell
    - Flywheel
    - Battery storage
    - Vehicle to grid
    - Configurable converter models and topologies
  - Investigation of new operating strategies and protection
  - Investigation of coordination of new communication protocols (e.g. IEC 61850)
  - Microgrid and distributed generation (DG) studies
- AC system studies
  - System security and transient stability investigations
  - Electromagnetic transient studies
  - Wide area protection and control development and testing
  - Black start

- Islanding and anti-islanding

- Academics
  - Masters and PhD projects
  - Hands-on exposure to physical protection and control equipment in a realistic power system environment
  - Demonstration of real-time dynamic responses (such as machine swings) to students to re-enforce class room theory
- Marine electrical
  - Conventional ship simulations
  - All electric ship simulations
    - AC schemes
    - DC schemes
    - Hybrid schemes
    - Pulse loads

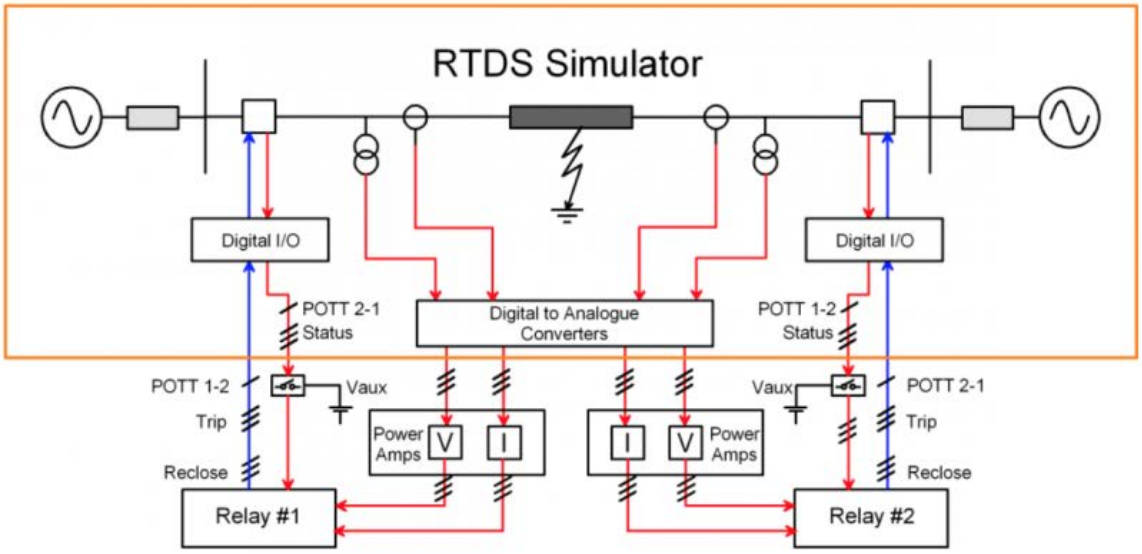
- Power Hardware In the Loop (PHIL)
  - Microgrid research
  - Analysis of physical DG such as PV, fuel cell, wind, energy storage, etc.
  - Power equipment testing
    - Mechanical
    - Electrical

## 2.1 PROTECTION SYSTEMS TESTING

The RTDS Simulator offers the most advanced and effective means available for testing protection systems. Since the simulation runs in real time, the physical protection equipment can be connected in closed-loop with the power system model.

The controlled and flexible environment of the digital simulation allows protection equipment to be subjected to virtually all possible faults and operating conditions. The closed-loop interaction of the protection system with the network model provides insight on both the performance of the relay scheme as well as its effect on the power system.

As is illustrated below, a model of the power system is implemented on the RTDS Simulator that includes the high voltage components (e.g. lines, breakers, instrument transformers, power transformers, generators, etc.) plus the required protection and control functions not included in the equipment under test.

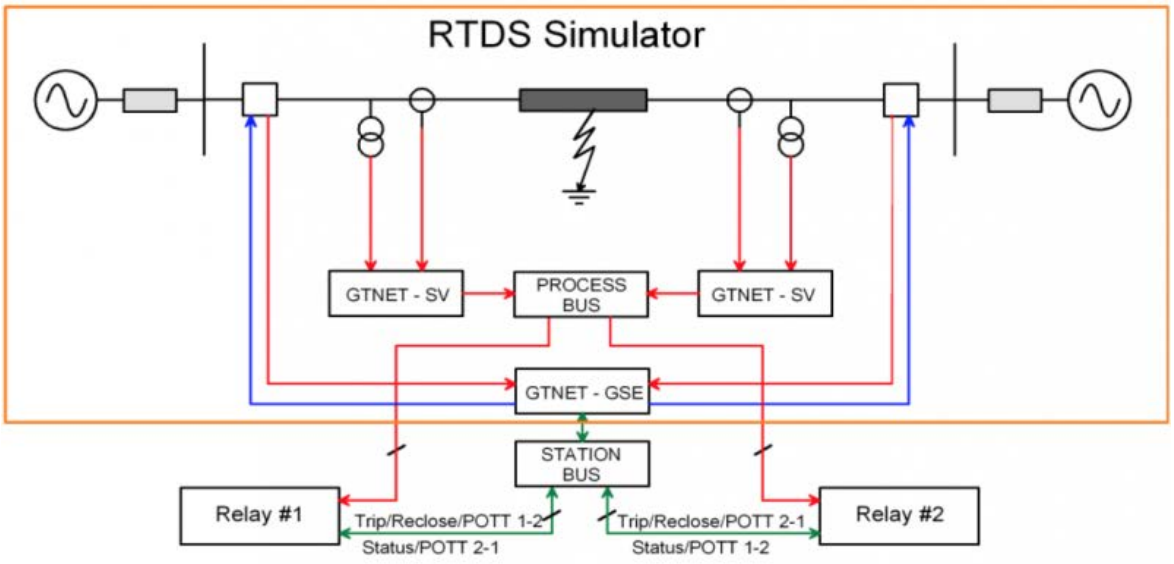



*CONVENTIONAL PRTOTECTION TESTING*

Typically, detailed models of the instrument transformers (CTs, PTs and CVTs) are used to provide signals to digital to analogue (D/A) converters. These signals are proportional to the secondary voltage and current signals the protection equipment would see in service. Including the instrument transformers in the model makes it possible to evaluate their effect on the performance of the protection system. Alternatively, the primary voltage and current signals can be sent directly to the protection equipment using the appropriate scaling factor.

The analogue output of the RTDS Simulator is provided by the GTAO card, which utilizes 16-bit D/A converters and allows high accuracy gain and offset calibration. The GTAO operates over a maximum range of +/- 10 Vpeak. To provide secondary voltage and current to the protection equipment, the GTAO output can be connected to power amplifiers that can accept low level voltage inputs. In some cases, however, the GTAO output can be connected directly to the protection equipment for "low level" testing, which bypasses the auxiliary current and voltage transformers inside the protection equipment.

When testing Sampled Values (SV) compliant devices, the GTAO card and power amplifiers can be replaced by the GTNETx2 or GTFPGA-SV card, running the SV network protocol. Both IEC 61850-9-2LE as well IEC 61869-9 protocols at various sampling rates are supported.




*IEC 61850 PROTECTION TESTING*

The protection should respond to faults by providing trip and possibly subsequent reclose signals. Since the network model is simulated in real time, the signals from the protection will be used to operate breakers modelled in the simulation. The simulated breaker models can include the mechanical operating time (either fixed or statistically varied) and provide breaker status.

There are several ways for the breaker commands to be imported into the real time simulation from the protection equipment. If the protection provides signals via conventional dry contacts they can be input either via a Low Voltage Digital Input/Output Interface Panel (controlled by a GTFPI card) which are included with the RTDS cubicle (no additional hardware is needed), or a GTDI card.

The breaker commands available in the RTDS Simulator are used to open and close the breakers (3 pole or single-pole). Depending on the type of protection being tested, it may be necessary to send the breaker status out of the Simulator to the protection equipment. Breaker status can be provided to conventional relays using the 250 Vdc Digital Output Interface Panel which includes dry contacts controlled by the simulation. The dry contacts included on the 250 Vdc Digital Output Interface Panel are solid state devices that operate in less than 0.2 ms and can accommodate any voltage level to a maximum of 250 Vdc. The 250 Vdc Digital Output Interface Panel is an additional piece of hardware that can be outfitted on the Simulator cubicle if desired.

If the protection equipment is IEC 61850-compliant, the trip, relcose, and status commands can be exchanged between the protection equipment and the simulation via GOOSE messaging using the GTNET-GSE protocol.

Binary communication between protection equipment (e.g. POTT schemes) can be transferred through the RTDS Simulator so that the signal delay can be included in testing. Therefore, coordinated protection schemes can be tested using the RTDS Simulator to observe interaction between the components of the protection system (e.g. between different relays) and between the protection and the power system.

With the real time simulation and the protection equipment connected in closed-loop, the protection device can be subjected to a myriad of faults and operating scenarios. Each condition can easily be repeated to investigate misoperations or test the equipment stability.

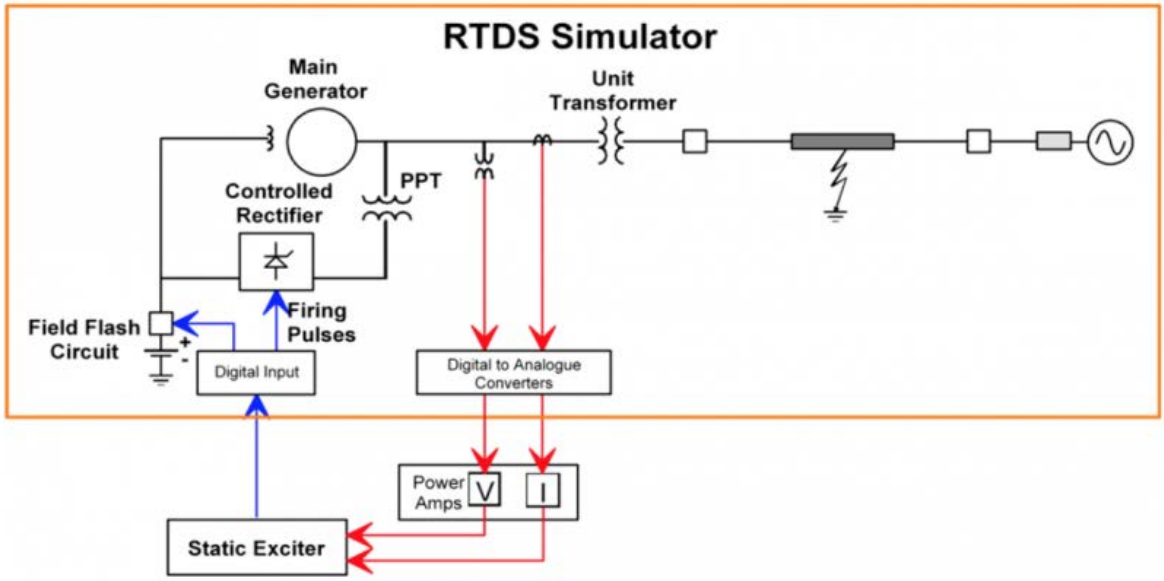
The faults and operating scenarios can be run manually from the RunTime console or using the automated batch mode facility. The automated batch mode facility is often applied to protection system testing where faults are repeated again and again with small changes to the fault inception angle, fault type, fault location, etc. These cases can all be run automatically controlled by C-like script implemented with the automated batch mode facility. Scripts can even record, store, print and evaluate results. The results can be saved in RSCAD MultiPlot, COMTRADE, jpg or pdf format. Key data from results (trip times, max/min values, etc.) can be stored in ASCII or MS Word/Excel report files.

## 2.2 CONTROL SYSTEMS TESTING

The RTDS Simulator is the ideal tool for testing of power system controls where real time closed-loop interaction between the power system simulation and the control hardware is essential.

The real time digital simulation environment provided by the RTDS Simulator allows the controls to be subjected to everything from steady state to rare emergency operating conditions. All conditions created can quickly and easily be repeated to investigate, understand, and optimize the control behavior.

Since the simulation runs in real time, the physical control equipment can be connected in closed-loop with the power system model. The closed-loop interaction of the control system and the network model provides insight on both the performance of the control scheme as well as its effect on the power system.




*HARDWARE IN THE LOOP TEST*

As illustrated, a model of the power system is implemented on the RTDS Simulator that includes the high voltage components (e.g. power electronics, generators, filters, lines, breakers, power transformers, etc.) plus the required protection and control functions not included in the equipment under test.

The controls are connected to the real time simulation using the input/output (I/O) components provided with the RTDS Simulator. Analogue output signals (representing various voltages, currents, etc.) sent from the simulator to the controls are typically provided by the GTAO card which operates over a maximum range of ± 10 Vpeak. The GTAO output is updated a minimum of once per timestep. If the simulation signal is sent from a standard timestep model, typically in the range of 50 µs, an option is provided to oversample the output through linear interpolation at a rate of 1 µs thus reducing the time between updates of the analogue output. If the simulation signal is generated by a small timestep subnetwork (typically running with a timestep in the range of 1.5 – 3 µs), the GTAO output will be updated once every small timestep.

Digital output signals (e.g. breaker status, tap position, etc.) from the Simulator to the controls are provided by the GTDO card and/or the dry contacts included on the 250 Vdc digital output interface panel.

Analogue input signals are passed from the controls to the simulator with the GTAI card. Analogue inputs are sometimes used as control signals in the simulation, but in some instances are simply imported for data acquisition purposes. The GTAI input can be read into either the standard timestep area or into a small timestep subnetwork and are sampled every 1 µs.

Digital input signals from controls are typically brought into the simulation through the GTDI cards. The GTDI input circuit an opto-coupler that turns on with a current of approximately 10 mA. Therefore, any input voltage level can be accommodated through the use of an appropriately sized current limiting resistor. The GTDI input can be utilized in either the standard or small timestep areas and the status is passed into the simulation every timestep, large or small. However, if the GTDI input is a firing pulse for a line commutated device (i.e. thyristor), the Digital Input Time Stamp (DITS) function can be used to improve the firing pulse resolution. The DITS function works by having the GTDI sample the input every 250 ns. If the input is activated at any point during the timestep, the GTDI card timestamps the arrival of the firing pulse. The DITS information is passed to the valve group model and is used to provide an effective interpolation of the firing pulse instant and allows a continually variable firing instant to a resolution of approximately 1 µs. The DITS function is very important when modelling LCC-based HVDC, SVC, and TCSC schemes.

## 2.3 HVDC AND FACTS

HVDC and FACTS devices are among the critical technologies used to ensure and enhance the controllability, reliability, and safety of modern power networks. The RTDS Simulator was originally developed to model HVDC schemes, and over the last two decades the Simulator has revolutionized the testing process of HVDC and FACTS devices. Today, it is the ideal tool for the simulation and testing of HVDC and FACTS devices. RSCAD includes a wide variety of sample cases, including MMC (Modular Multilevel Converter) HVDC, SVC MMC, and LCC HVDC schemes, among others.

All of the major manufacturers use the RTDS Simulator to test their HVDC/FACTS controls during Factory Systems Testing. Systems successfully tested include LCC- and VSC-based HVDC and UHVDC, modular multi-level converters, network and industrial SVCs, STATCOMs, TCSCs, DVRs, UPFCs, and more.

Many electrical utilities around the world have also purchased RTDS Simulators to connect to replica controls for HVDC and FACTS projects. In these cases, a slightly simplified copy of the controls is delivered to site along with an RTDS Simulator to represent the power system. These "replica Simulators" are then interfaced with the controls and are generally used to investigate proposed network changes and control modifications, to test scheme upgrades and refurbishment, and to train utility personnel on scheme theory and operation. A few notable utility projects are listed here for reference.

**Operador Nacional do Sistema Elétrico (ONS):** This Brazilian utility is responsible for the coordination and control of the Rio Madeira HVDC link. At 2,375 km long, it is the longest transmission link in the world. The controls for this project were tested exclusively on the RTDS Simulator.

**Trans Bay Cable:** Located in the San Francisco Bay Area, this energy transmission company owns and operates the Trans Bay Cable, an 85 km submarine HVDC cable which transfers energy from the City of Pittsburg to the City of San Francisco. This was the world's first ever HVDC project to use an MMC system, and was tested using the RTDS Simulator.

**Power Grid Corporation:** This Indian utility is responsible for the North-East Agra (NEA) link – the world's first ever multi-terminal UHVDC transmission link. Once commissioned, NEA will transmit clean hydro power from the northeast region of India to the city of Agra. The link includes four terminals in three converter stations with a total converter capacity of over 8,000 MW – the largest HVDC transmission system ever built. This project was tested using the RTDS Simulator.

The small timestep library of RSCAD contains an extensive selection of HVDC- and FACTS-related components. RSCAD's small timestep subnetworks operate with timesteps in the range of 1-3 µs and can be interfaced to large scale simulations operating with timesteps in the order of 30-50 µs. A key feature of these subnetworks is that the circuit and valve topology is user configurable. Two- and three-level converters can be freely configured to provide crow-bar circuits, etc. for PWM switching rates greater than 2 kHz. A low-loss, fixed topology two-level sub-step converter is also available for operation at PWM switching frequencies of up to 40 kHz. Multiple small timestep subnetworks can be linked together by traveling wave transmission lines or cables to create entire systems running with timesteps of 1-3 µs.

The development team at RTDS Technologies is always working on improving existing models and adding new models to RSCAD. Currently, the RSCAD model library includes the following:

**LCC Models:** RSCAD contains both six- and twelve-pulse LCC valve group models. The models support a broad range of valve faults, both between internal nodes and also to external nodes. These can be easily configured to represent UHVDC (i.e. with several series groups) and allow faults to points both internal and external to the converter. The improved firing algorithm is used to allow the converters to represent a continually variable firing instant with an accuracy of 1 µs.

**VSC/MMC Models:** Two- and three-level converter models, including point-to-point and back-to-back schemes, are available. RSCAD also includes several MMC models. MMCs offer many advantages over conventional thyristor-based schemes and are increasingly popular for HVDC and FACTS applications. Their inherent complexity also presents challenges for modelling with EMT simulation techniques. The RTDS Simulator offers the most advanced means available for the simulation and testing of MMC schemes, and is equipped with a number of models which

overcome these challenges. The MMC models available for the RTDS Simulator are described in the section below.

**Firing Pulse and Ramp Generators:** High resolution firing pulse words can be produced in the small time-step code through use of firing pulse generation blocks available in the library. They can also be brought into the simulation directly from a GTDI digital input card.

The RTDS Simulator features two main types of MMC models: core-based MMC models, which are executed on cores within the NovaCor chassis, and FPGA-based models, which are executed on the GTFPGA-MMC Unit. These models are suited for a variety of applications from high level controls and system performance testing to detailed control algorithms, and are described below.

**Generic Model (FPGA-based):** The Generic Model (GM) can be used to represent up to 2 valve legs on one MMC Support Unit V2. Each valve leg can include up to 512 submodules. Both half and full bridge configurations are supported. All possible IGBT firing states are considered. The GM supports individual IGBT firing, individual submodule capacitances, customized topologies, and additional internal faults. Additional GM models are available for internal node to ground faults as well as mixed half and full bridge configurations.

**Unified Model (FPGA-based**): The Unified Model (U5) can be used to represent up to 6 valve legs on one GTFPGA-MMC Unit. Each valve leg can include up to 512 submodules. Both half and full bridge configurations are supported. Normal firing states (blocked, positive inserted, negative inserted, and bypassed) are considered. Internal faults can be simulated, but not at the individual IGBT level.

**MMC5 (core-based):** The MMC5 component is designed for the testing of high level controls and system performance. Six valve legs can be simulated on one core. Each valve leg can have up to 640 submodules. Both full and half bridge configurations are supported. Ideal capacitor voltage balancing is provided internally by the model. At the end of each small timestep, all submodules arrive at the same capacitor voltage.

**CHAINV5 (processor-based):** The CHAINV5 is a core-based model that supports individual submodule firing pulse input, and can be used to test detailed firing pulse controls. CHAINV5 can model 40 submodules per valve for a full bridge configuration, or 56 submodules per valve for a half bridge configuration. The simulation of internal faults is not permitted when using CHAINV5.

## 2.4 PMU/WIDE AREA PROTECTION AND CONTROL STUDIES

Phasor measurement unit (PMU) studies can be achieved using the GTNETx2 card with the flexible PMU firmware.

PMUs can be an embedded function within relays or disturbance recorders, or alternatively they can be standalone products. RTDS simulations can include PMU models, allowing the PMU data to be used for the monitoring of oscillations, angle difference, system frequency, voltage stability and other variables. Other ideas for PMU data include situational awareness, alarm and operational limit settings, state estimation and congestion management – to name just a few.

Generally, the PMU is simulated within RSCAD, and the IEEE C37.118 data streams are sent to a phasor data concentrator (PDC) or other control/protection equipment which are external to the simulator. This is accomplished using the PMU firmware option for the GTNETx2 card, which provides synchrophasor output data streams according to the IEEE C37.118 standard.

The GTNET-PMU component output is synchronized to an external 1PPS, IRIG-B or IEEE 1588 signal via the GTSYNC card.

**PMU TEST UTILITY**

The PMU Test Utility available in the RSCAD software is designed for testing the steady state and dynamic performance of PMUs. The IEEE C37.118 standard and its amendments define test signals and performance limits that must be met to adhere to the standard and the IEEE Conformance Assessment Program (ICAP) has defined a Test Suite Specification (TSS) that addresses specific test procedures and calculations. The PMU Test Utility is designed to run the test procedures and calculations defined by the ICAP-TSS.

The PMU Test Utility is used to set the various parameter sliders that are embedded in the PMU waveform control component in RSCAD. The resultant waveforms are then sent to a GTAO card and appropriately scaled for connection to amplifiers or low level direct connections to the PMU under test. The slider values are also used by the PMU utility to calculate the theoretical phasor values for each test.

The PMU Test Utility then gathers the measurements made by the PMU and displays them for analysis. The measured phasor, frequency, and ROCOF values are then compared to the theoretical values, and calculations such as frequency error, ROCOF error, and total vector error (TVE) are made.

A GTSYNC card must be used for these tests in order to synchronize data to an external 1PPS, IRIG-B, or IEEE 1588 signal.

## 2.5 SMART GRID & RENEWABLE ENERGY

The RTDS Simulator has been under constant development for over 20 years in order to keep up with the always-evolving power industry. Recently, the concepts of smart grid and distributed generation are gaining immense speed on a global scale. Equipment manufacturers, utilities, universities and research institutions worldwide are endeavoring to develop solutions that mitigate our impact on the environment, strengthen the security and reliability of our energy infrastructure, and ensure the efficient generation, transmission and distribution of electricity. RTDS Technologies strives to keep its product cutting-edge and current. Therefore, the RTDS Simulator is capable of simulating many smart grid- and renewable energy-related concepts.

The term "smart grid" refers to an evolved electrical grid that uses communications technology to gather and respond to information in order to manage electricity in a more reliable, secure and sustainable manner. "Smart grid" doesn't refer to a specific technology, but rather, the suite of technologies and operating procedures that will revolutionize the grid.

The implementation of smart grid technology in the real-time simulation environment requires high-level communication capabilities. Using the GTNET or GTNETx2 card and its available firmwares, the RTDS Simulator is capable of the following smart grid-related communication:

- IEC 61850 for substation automation applications
- DNP and IEC 60870-5-104 for SCADA systems
- IEEE C37.118 for PMU applications

The RTDS Simulator also has facilities and models for simulating distributed generation and renewables. Wind turbines, photovoltaics, fuel cells, batteries and various other power sources can be represented by library components, while the corresponding power electronics, including VSC converters, can be freely configured in small timestep subnetworks.

## 2.6 POWER ELECTRONICS

Many power electronics-based schemes require small timesteps to properly represent high frequency switching and circuit dynamics. To efficiently include such schemes in larger scale simulations, RTDS Technologies has developed the small timestep subnetwork technique.

The subnetworks operate with timesteps in the range of 1-3 µs and can be interfaced to large scale simulations operating with timesteps in the order of 30-50 µs. A key feature of subnetworks is that the circuit and valve topology are user configurable. Individual switching elements are available so converters can be freely configured to provide crow-

bar circuits, etc. for PWM switching at greater than 2 kHz. In addition, users can choose from fixed-topology converters (2, 3, multilevel). A low-loss, fixed topology two-level converter is also available for operation at PWM switching frequencies in the range of 40 kHz.

Multiple small timestep subnetworks can be linked together by traveling wave transmission lines or cables to create entire systems running with timesteps of 1-3 µs.

There are a variety of components available in the small timestep component library of the RSCAD software, including transformers, induction and synchronous machines, transmission lines and cables, high accuracy signal generators, and HVDC valve groups.

## 2.7 POWER HARDWARE IN THE LOOP

Power Hardware In the Loop (PHIL) simulation involves the real-time simulation environment exchanging real and reactive power with physical power hardware, such as renewable energy devices, electric vehicles, batteries, motors, loads, etc.. The RTDS Simulator has been successfully used for performing PHIL experiments in a wide range of applications.

Here are a few examples of PHIL projects that have been carried out by RTDS Simulator users:

- The testing of motors of electric ships and motor drives in the MW range
- Virtual Synchronous Generator (VSG) testing
- The testing of motors of electric ships and motor drives in the MW range
- Virtual Synchronous Generator (VSG) testing
- Testing of variable-speed wind turbine generators in the MW range
- Three-phase power converter synchronization study
- Photovoltaic inverter (PV) testing

PHIL simulation enables the real time testing of devices in a controlled environment before they are connected to the actual physical system. A software model of the actual system where the physical device will operate is developed on the RTDS Simulator, and voltage and current signals are exchanged with the device. The interface between the RTDS Simulator and the device under test should be carefully considered with respect to the computation time step of the RTDS Simulator, as well as the delay introduced from the amplifiers and transducers, which all determine the total delay in the PHIL interface. This interface device must be capable of both sourcing and absorbing both real and reactive power and is referred to as a 4 quadrant power amplifier. The method used to exchange the voltage and current signals in the PHIL interface and the power ratings of the test device and selected amplifier are also critical considerations.

Typically, during a PHIL study, digital to analogue converters included as part of the RTDS Simulator (via the GTAO card) provide analogue signals scaled down to electronic levels within ±10Vpk. These signals are provided as input to an amplifier which provides the required voltage or current level to the device under test. Sensors measure the voltage or current signals obtained from the device under test, which are then passed through an analogue to digital converter (via the GTAI card) and sent back to the RTDS Simulator to close the loop. Filters implemented in hardware/software are required to eliminate noise in the PHIL interface. The filter design and parameters should be selected to offer an acceptable trade-off between improved stability and reasonable accuracy of the PHIL simulation.

### 2.8 EDUCATION AND TRAINING

**EDUCATIONAL ENVIRONMENT**

Many universities and other learning institutions worldwide have incorporated the RTDS Simulator into their education and R&D programs. Programs involving the RTDS Simulator have been set up for students at the undergraduate and postgraduate levels.

Students can effectively interact with an operating power system modelled by the Simulator. The RTDS Simulator provides the students with a hands-on illustrative tool to help them bridge the gap between theory and practical operation of a power system. The real time operation of the simulator also allows students to gain experience with real measurement, protection and control equipment which can be connected to the RTDS Simulator.

A full set of sample manuals for undergraduate laboratories which employ the RTDS Simulator is available upon request.

**OPERATOR TRAINING ENVIRONMENT**

Utilities worldwide use the RTDS Simulator to represent their network and train operators. The Simulator allows engineers and technicians to work with and test utility-specific physical protection and control equipment – under live operating conditions. Changes and modifications can be executed and tested in a safe laboratory environment before being implemented in the field.

Our utility customers have reported that the utilization of the RTDS Simulator for training purposes has resulted in reduced system downtime, the prevention of equipment damage, a more favourable reputation with their customers, and residual increased revenue.

## 3 RTDS SIMULATOR OVERVIEW

The most common and most robust solution employed by electromagnetic transient simulation software (PSCAD, ATP, EMTP, etc.) is the Dommel Algorithm. In this algorithm,

the trapezoidal rule of integration is used to convert integral equations, which result from nodal analysis of the power system, into algebraic equations. Application of the trapezoidal rule requires that the solution be computed only at discrete instants in time, rather than a continuous solution. The time between computed instants is known as the timestep and is denoted $\Delta t$.

All of the equations representing the circuit model must be computed in each timestep. For large and complex power system models involving power electronics, it may take a modern computer many seconds to compute even a single timestep. In this case, the simulation is said to operate in "non real time" or "off-line" mode. However, if the computer is able to continuously perform the necessary calculations for a single timestep, in a measured time less than or equal to the timestep, the simulation is said to operate in real time. Furthermore, if the system is able to perform the simulation in real time and exchange data with the outside world at constant intervals equal to the simulation timestep, it is said to operate in "hard real time".

The RTDS Simulator is a fully digital system capable of performing electromagnetic transient simulations using the Dommel algorithm, continuously in real time operation. The simulator allows for multi-rate simulations with timesteps from 1.5 - 50 microseconds utilizing a combination of custom software and hardware. The proprietary operating system used by the RTDS Simulator guarantees "hard real time" during simulations and does not allow any calculation overruns.

The RTDS Simulator is easy and efficient to use since all aspects of a simulation are controlled via the simulator software, RSCAD. RSCAD provides a graphical interface for setting up simulations, controlling operation, modifying system parameters during a simulation, data acquisition, and analyzing simulation results. RSCAD also includes comprehensive libraries of power system and power electronic component models, control system components, as well as protection and automation component models that can be used to create detailed simulation cases. These models have been designed and tested by the development team at RTDS Technologies and validated and refined by clients during their daily work with the simulator.

The RTDS Simulator hardware utilizes a modular design; enabling expansion of the simulator's computing power and I/O capabilities at any time. Additional core licenses (up to a maximum of 10 cores per chassis) or chassis can be added to the simulator at any time. The current design allows as many as 60 chassis to be connected to form one simulator. The I/O cards described below in the Optional Equipment section can also be added at any time. Each NovaCor chassis has 24 optical fibre ports that the I/O cards can be connected to. Multiple I/O cards can also be connected to one GT port in a daisy chain (series) configuration.

The RTDS Simulator is an ideal tool for thoroughly designing, studying, and testing physical equipment such as protection and control schemes. With massive analogue/digital/Ethernet I/O capabilities, physical protection and control devices can be connected to the RTDS Simulator to interact with the simulated power system during closed-loop testing.

The role the RTDS Simulator can play in the training of operators, engineers, researchers, and students is diverse. Inherently, work on the simulator introduces techniques and advantages of simulation, with particular relevance to the electrical power industry. Since the simulator operates continuously in real time, it will serve to provide a "feel" for the operation and behavior of real power systems. Measuring devices, protective relays, and controllers can be connected to the simulated system providing an opportunity to operate them under "real life" conditions. The user has the opportunity to configure and operate the circuit models and to study the interaction between simulated circuit and the hardware under test.

# 4 RTDS SIMULATOR HARDWARE

The RTDS Simulator hardware is designed specifically to solve the Dommel Algorithm for Electromagnetic Transients in real time. By nature, the Dommel Algorithm allows two levels of parallel processing:

- Parallel processing of components connected to a common admittance matrix (i.e. within one subsystem)
- Parallel processing of subsystems (i.e. decoupled admittance matrices)

The RTDS Simulator mimics the first level by using the tightly coupled cores of a processor within a chassis to solve components connected to a common admittance matrix. The second level is implemented by using separate chassis to solve different simulation subsystems (communicating via dedicated gigabit per second communication channels). The second level of parallel processing, allows virtually limitless expansion of the system.

In addition to being designed to execute the Dommel algorithm in real time, the RTDS Simulator was designed to test physical protection and control equipment. One of the main considerations of testing physical devices is the Input/Output structure. To maximize the communication bandwidth and minimize the time required, the RTDS was designed to provide the most direct route possible for I/O to be passed from the processors performing the simulation to the I/O channels. Providing multiple I/O communication paths for each processor avoids possible communication bottlenecks.

## 4.1 NOVACOR

Each unit of the RTDS Simulator hardware is referred to as a NovaCor chassis. Each chassis contains a powerful multi-core processor, Workstation InterFace (WIF) functionality, communication ports, and analogue output channels.


*NOVACOR CHASSIS*

### *4.1.1 PROCESSOR*

Each NovaCor chassis contains an IBM POWER8™ RISC processor with 10 cores, operating at 3.5 GHz. These 10 cores are used to solve the overall network solution, auxiliary components (i.e. lines, machines, transformers, etc.), as well as any controls present in the simulation.

The NovaCor is extremely modular. Individual cores can be licensed so as few as 1 core or as many as 10 cores can be applied to solve a particular circuit within a given chassis. Multiple NovaCor chassis can be used for simultaneous, parallel simulations, or they can be connected together so their combined power can be used to solve larger networks.

### *4.1.2 CAPABILITIES*

Each NovaCor chassis can model up to 600 single-phase nodes (200 three-phase buses) split over two network solutions as well as component models with additional embedded nodes. Control components are typically solved on the same core(s) as the network solution(s) while the remaining licensed cores can be dedicated to solving component models (lines, machines, etc.) or small timestep subnetworks. Additional licensed cores can also be used to model control components if the computational burden causes the simulation timestep to reach unacceptable limits.

A NovaCor chassis with one core licensed is capable of modelling up to 90 single-phase nodes (30 three-phase buses) plus power and control system components.

### 4.1.3 *INPUT / OUTPUT*

Each NovaCor chassis includes 12 isolated, 12-bit digital to analogue converters (D/As). The D/A output range is +/- 10 Vpeak. These D/A channels are primarily used for real time monitoring of simulation variables.

Each NovaCor chassis has 24 optical fibre ports that can be used interchangeably for connecting to the modular I/O cards. Conventional analogue and digital I/O cards are typically mounted on rails in the back of the simulator cubicle while the GTNETx2 cards used to provide Ethernet-based communication are installed in a dedicated chassis mounted in the cubicle. All of the I/O cards are described in detail below under the Optional Equipment section.

### 4.1.4 *WORKSTION INTERFACE (WIF)*

The WIF functionality is provided on NovaCor to handle communication requests between the chassis and the host computer running RSCAD. Each NovaCor chassis contains an Ethernet transceiver and is assigned its own static Ethernet (IP) address, thus allowing connection to any standard Ethernet-based Local Area Network (LAN). All of the low level communication requests between the simulator and the host computer are handled by the high level software running on the host computer and the operating system being run on the NovaCor. The communication medium used between the NovaCor chassis and the host computer is a standard Ethernet (100/1000baseT) TCP/IP-based LAN.

*NOVACOR-PC CONNECTION*

From a hardware level, the NovaCor chassis is seen as a specialized computer available on a LAN. Any computer connected to that network can access the simulator.

### 4.1.5 *SYNCHRONIZATION*

All cores within a chassis are inherently synchronized since they are part of a single processor. When an RTDS Simulator consists of more than one chassis, a "Global Bus" signal is provided from one chassis to synchronize the calculations of all cores on all chassis. An RTDS Simulator consisting of a single chassis operates independently while a two chassis RTDS Simulator can operate by making a direct Global Bus connection between the chassis. For simulators with 3 chassis or more, each chassis connects to a Global Bus Hub (GBH) using a fibre optic Tx/Rx cable. The fibre optic cables connecting the chassis to the GBH can have a maximum length of 30 m.


*NOVACOR-GBH CONNECTION*

The GBH synchronization signal is separate from the Ethernet communication used to exchange information between NovaCor and the host workstation.

### *4.1.6 COMMUNICATION BETWEEN NOVACOR CHASSIS*

When a simulation is split over multiple chassis, dedicated communication paths known as Inter-Rack Communication (IRC) channels are used to pass simulation data between chassis. Each NovaCor chassis has 6 IRC channels for direct point-to-point communication between up to 7 chassis. If the simulator has more than 7 chassis, an IRC Switch may be used to enable direct communication between as many as 60 chassis in a star configuration.

In a multi-chassis simulation, equations representing different portions of the network can be solved in parallel on different chassis and the required data can be exchanged between them via the IRC communication channels. Thus, an RTDS Simulator can be comprised of many chassis and be used to simulate very large networks while still maintaining real time operation.

The IRC links between the NovaCor chassis or between the chassis and the IRC Switch are provided by optical fibre. The fibre optic cables for the IRC channels can have a maximum length of 30 m.

The NovaCor IRC communication channels are dedicated and are not to be confused with either the GBH connections or the Ethernet communications between the host computer and the RTDS Simulator.

## 4.2 OPTIONAL EQUIPMENT

It may be necessary when interfacing the RTDS Simulator to external equipment (e.g. relays or controls) to use the optional equipment described below to provide isolation and/or make the connection more convenient and more accurate.

### 4.2.1 GTAO – (Gigabit-Transceiver Analogue Output) Card

The GTAO is a rail mount card that provides optically isolated analogue output from the simulation via a connection to a NovaCor optical port. The card has a total of 12 outputs which can be sent from either a regular or small timestep simulation running on the NovaCor. Special care has been taken in the design of the GTAO to provide the accuracy and settling time required for the small timestep applications. The GTAO allows a daisy chain connection so that numerous GTIO cards can be driven from one NovaCor optical port.

The GTAO output can range between a maximum of ± 10Vpeak.

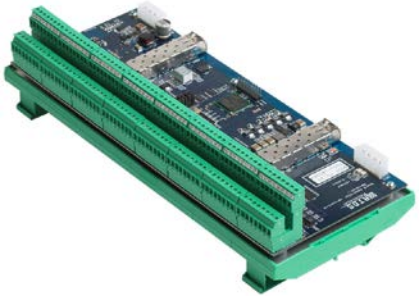
When operating with a regular timestep simulation, the GTAO card can provide oversampling of the output at 1.0 µs.

### 4.2.2 GTAI – (Gigabit-Transceiver Analogue Input) Card

The GTAI is a rail mount card that provides optically isolated analogue input from the simulation via a connection to a NovaCor optical port. The card has a total of 12 inputs for use with components running on the NovaCor. The GTAI allows a daisy chain connection so that numerous GTIO cards can be driven from one NovaCor optical port.

The GTAI input can range between a maximum of ± 10Vpeak.

### 4.2.3 GTDI – (Gigabit-Transceiver Digital Input) Card

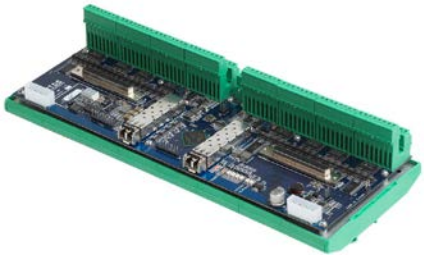


The GTDI is a rail mount card that provides optically isolated digital input to the simulation via a connection to a NovaCor optical port. The card has a total of 64 inputs for use in regular or small timestep simulations running on the NovaCor. The GTDI allows a daisy chain connection so that numerous GTIO cards can be driven from one NovaCor optical port.

The GTDI inputs are current driven (~10mA), allowing a wide range of input voltages to be connected to the card when the appropriate value of current limiting resistor is provided. 5V and 24V SIP resistors are provided standard with each GTDI card

The GTDI card can also provide Digital Input Time Stamp (DITS) functionality for improved firing of regular timestep valve groups.

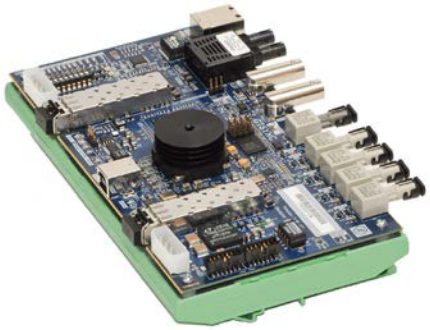
### 4.2.4 GTDO – (Gigabit-Transceiver Digital Output) Card



The GTDO is a rail mount card that provides optically isolated digital output from the simulation via a connection to a NovaCor optical port. The card has a total of 64 outputs which can be sent from either a regular or small timestep simulation running on the NovaCor. The GTDI allows a daisy chain connection so that numerous GTIO cards can be driven from one NovaCor optical port.

The GTDO has a source driven output that can range from +7 to +24 V.

### 4.2.5 GTSYNC – (Gigabit-Transceiver Synchronization) Card



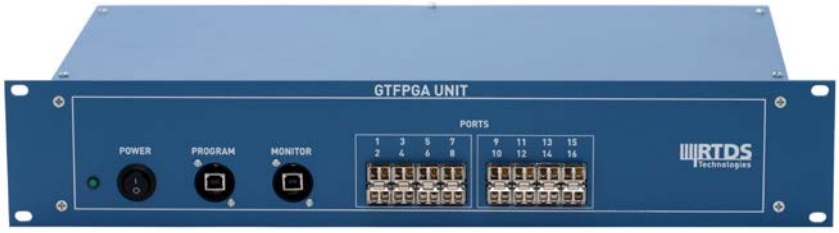
The GTSYNC card is a rail mount card that allows the simulation timestep to be synchronized to a 1 Pulse Per Second (1PPS), IEEE 1588 or IRIG-B time reference signal provided by an external time reference (e.g. GPS clock). Alternatively, the GTSYNC can act as the master time reference, generating either 1PPS or IRIG-B. An IRIG-B signal must be connected to the GTSYNC using the BNC coax cable connector, while the 1PPS signal can be connected using either the BNC coax cable connector or the ST style fibre optic connector. The IEEE 1588 synchronization is performed over Ethernet using 100BASE-TX via RJ45 connector or 100BASE-FX via ST style fibre optic connectors. Regardless of whether the timing source is external or internal, and regardless of what the source protocol is, the GTSYNC can provide 1PPS or IRIG-B outputs.

The synchronization signal provided by the GTSYNC is connected to a NovaCor optical port to act as the master for the simulation. The master in turn provides the synchronized timestep clock to the other NovaCor chassis via the Global Bus Hub (GBH) or directly for two chassis simulations.

Synchronization of the simulation timestep to an external time reference is necessary for Phasor Measurement Unit (PMU) benchmark testing and Sampled Values output.

### 4.2.6 GTFPGA Unit

The GTFPGA Unit is a rack mountable housing containing a Xilinx Virtex 7-based FPGA board that connects to the simulation via a NovaCor optical port. Depending on the firmware installed, the unit is used for a number of different purposes: modelling of MMC-based valves, MMC-based capacitor voltage balancing and firing pulse control, IEC 61850-9-2LE/IEC 61869-9 Sampled Values data streaming, and the modelling of small timestep frequency dependent transmission lines and cables. The FPGA board can also be used as a generic interface to the RTDS Simulator by using the GTFPGA netlist.




*GTFPGA-MMC*
Each GTFPGA-MMC can model six valve legs based on the U5 model or two valve legs based on the GM model.

When operating as the capacitor voltage balancing and firing pulse control, the GTFPGA-MMC can be configured to control three valve legs with a maximum of 768 submodules each. Therefore, one GTFPGA-MMC Unit would be required for control of a 3-phase STATCOM or two GTFPGA-MMC units to control one terminal of an MMC-based HVDC scheme.

Please see the HVDC and FACTS application section for more information on the available FPGA-based MMC models.

*GTFPGA-SV*
The GTFPGA-SV can provide up to 16 x IEC 61850-9-2LE or IEC 61869-9 streams at various sample rates with <1 µs jitter between samples.

For IEC 61850-9-2LE, it is possible to have up to 16 data streams for up to 4 current and 4 voltage channels, at a rate of 80 samples/cycle (1 ASDU) or 256 samples/cycle (8 ASDU).

For IEC 61869-9, it is possible to have up to 16 data streams for up to 24 quantities, at a rate of 80 samples/cycle (1 ASDU), 96 samples/cycle (1 ASDU), or 4,800 Hz (2 ASDU). Alternatively, it is also possible to have 16 data streams for up to 9 quantities, at a rate of 256 samples/cycle (8 ASDU) or 14,400 Hz (6 ADSU)

The GTFPGA-SV requires a GTSYNC card for synchronizing the SV timestamps.

*GTFPGA-TLINE*
The GTFPGA-TLINE component can model as many as 12 frequency dependent, small timestep transmission line or cable conductors.

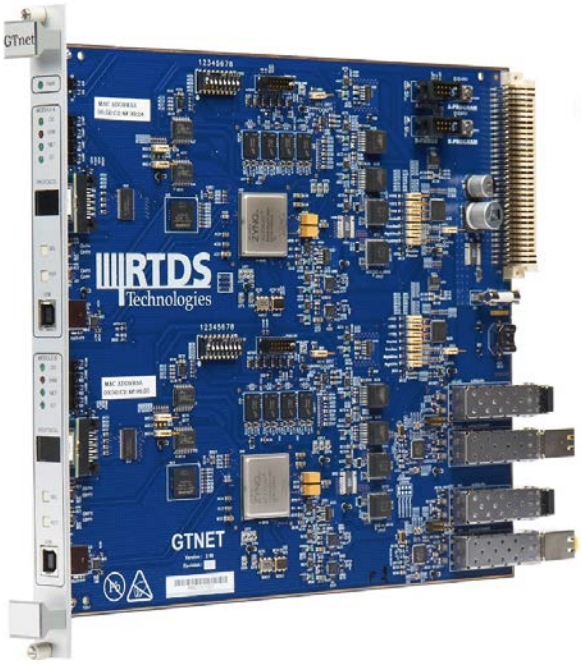
*GTFPGA-GENERIC*
If the GTFPGA Unit is used with the GTFPGA netlist, a link to a NovaCor can be established in either the large or small timestep domains. The function of the FPGA board can be programmed to facilitate an interface to external equipment or to create customized

models run on the FPGA board. Customized models run on the GTFPGA Unit must be programmed using VHDL code and Xilinx proprietary tools.

### *4.2.7 GTNETx2 – (Gigabit Transceiver Network Interface) Card*

The GTNETx2 card is the second generation of the GTNET™ card. It is used to interface network protocols with the RTDS simulator.

Unlike other I/O cards that are rail-mounted, GTNETx2 is mounted in a chassis, where it is powered by a backplane. Up to three GTNETx2 cards can reside in one chassis and additional chassis can be added to the cubicle as needed. The GTNETx2 card communicates information to and from a simulation the same as the other GTIO cards, via a connection to a NovaCor optical port.




Each GTNETx2 card has two modules. Each module has one Ethernet port, which may be equipped for one of three connection options: 100/1000 Copper, 100BASE-FX, or 1000BASE-SX. At the time of order, the customer shall specify their two desired Ethernet options.

Each module can have 1 active network protocol at any given time, which means each GTNETx2 card can operate a total of 2 network protocols simultaneously.


When a firmware is purchased, the license is specific to a module on the GTNETx2 card. The user can install as many of the presently available network protocols on the GTNETx2 card modules as they desire. Of all the installed protocols on a given GTNETx2 card module, the user can select 1 to be active at any given time.

Included in the purchase price of each GTNETx2 card are 2 network protocols – the new Socket ("GTNET-SKT") protocol, which is detailed below, and one additional user-selected

protocol. If the user wishes to install more than these 2 protocols on one GTNETx2 card, they must purchase the additional protocols separately.

*GTNET-SKT*
The Socket ("GTNET-SKT") protocol, which is included with the purchase of a GTNETx2 card, is used to interface with external software and physical equipment over a Local or Wide Area Network connection using Transmission Control Protocol (TCP) or User Datagram Protocol (UDP) sockets.

The communication is bidirectional and asynchronous. GTNET-SKT is capable of sending up to 300 data points per packet, with each point defined over 4 bytes. The data transmitted can be of either integer or floating-point (IEEE 754) type.

*GTNET-PMU*
The GTNETx2 provides a hardware link between a 10/100baseT Ethernet and an RTDS Simulation. The LAN connects to the GTNETx2 via a standard Ethernet cable and to the simulation via a NovaCor optical port. The PMU firmware option for the GTNETx2 provides synchrophasor output data streams according to the IEEE C37.118 standard. Two PMU streaming options are available for GTNET-PMU:

Using the first option, a single GTNET-PMU firmware can represent and provide output for up to eight (8) PMUs with symmetrical component information related to 3-phase sets of voltage and current using UDP or TCP connections. The frame rate of each PMU can be set individually between 1 and 60 frames per second. Frame rates as high as 240 frames per second are supported, but require the maximum number of PMUs represented by one GTNETx2 to be reduced from eight.

Using the second option, a single GTNET-PMU firmware can represent and provide output for up to twenty-four (24) PMUs containing only positive sequence data. Frame rates up to the system frequency (50/60 Hz) are supported.

The GTNET-PMU requires the use of a GTSYNC card.

*GTNET-GSE*
The GTNET-GSE firmware option for the GTNETx2 card can be used to model 1-4 individual IEDs (Intelligent Electronic Devices). Each IED is capable of sending and receiving up to 64 points (or 32 points with associated quality bitmap). For each GTNET-GSE firmware, GOOSE messages can be received from a total of 16 unique external IEDs. The GTNETx2 GOOSE configuration is done via an SCD file. RSCAD contains a built in SCD editor which helps the user to easily and conveniently configure the publication and subscription of GOOSE messages.

IEC GOOSE fields such as the Test mode, Needs Commissioning and individual Quality bitmaps can be dynamically changed and monitored for both transmit and receive messages during a simulation to allow many scenarios to be thoroughly tested and verified.

*GTNET-SV*
The GTNET-SV firmware option provides IEC 61850-9-2LE sampled value messaging for power system voltages and currents. The GTNET-SV can either publish or subscribe to sampled value data streams. The GTSYNC card is used to synchronize the SV timestamps with a precise time source, with <10 µs jitter between samples

With each GTNET-SV firmware, two data streams with up to 4 current and 4 voltage channels each can be transmitted at a rate of 80 samples/cycle. Alternatively, one data stream can be transmitted at 256 samples/cycle. It is also possible to receive 9-2LE data from one Merging Unit (4 currents and 4 voltages) at either 80 or 256 samples/cycle.

In non-9-2LE mode, based on IEC 61869-9 and the Chinese National Standard for SV merging units, one GTNET-SV can publish 1 data stream for up to 24 voltages or currents at a rate of 80 samples per cycle.

*GTNET-Playback*
The Playback firmware option for the GTNETx2 allows large COMTRADE files (many GBs) stored on a PC hard drive to be read by the GTNETx2. The GTNETx2 in turn passes the playback data to the NovaCor where it can be introduced into the simulation.

*GTNET-DNP*
The DNP firmware option allows the GTNETx2 to act as a DNP slave using the DNP 3.0 protocol. DNP is a very common SCADA communication protocol.

Using the DNP protocol, the GTNETx2 can accommodate the following maximum communication capacity:

- Binary status/output (i.e. breaker position) - 1024 (scan rate 1000 Hz)
- Binary control/input (i.e. breaker commands) - 512 (scan rate 1000 Hz)
- Analogue output - 500 (scan rate 4 Hz)
- Analogue input - 100 (scan rate 4 Hz)

The GTNET–DNP firmware supports one master with a maximum polling rate of less than 5 Hz.

*GTNET-104*
The 104 firmware option allows the GTNETx2 to act as a slave using the IEC 60870-5-104 protocol. IEC 60870-5-104 is a commonly used SCADA communication protocol.

Using the 104 protocol, the GTNETx2 can accommodate the following maximum communication capacity:

- Binary status/output (i.e. breaker position) - 1024 (scan rate 1000 Hz)
- Binary control/input (i.e. breaker commands) - 512 (scan rate 1000 Hz)
- Analogue output - 500 (scan rate 4 Hz)
- Analogue input - 100 (scan rate 4 Hz)

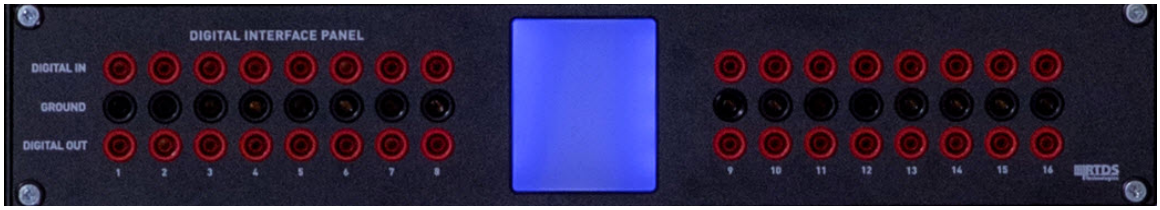
GTNET–104 firmware supports one master with a maximum polling rate of less than 5 Hz.

### *4.2.8 GTFPI – (Gigabit-Transceiver Front Panel Interface) Card*

The GTFPI card is a rail mount card that creates and receives TTL level digital electrical between the NovaCor and the Low and High Voltage panels. The signals are made available on interface panels typically located on the front of a simulator cubicle. All cubicles include at least one GTFPI card which can connect to one Low Voltage Digital Input/Output Interface Panel and one 250 Vdc Digital Output Interface Panel.

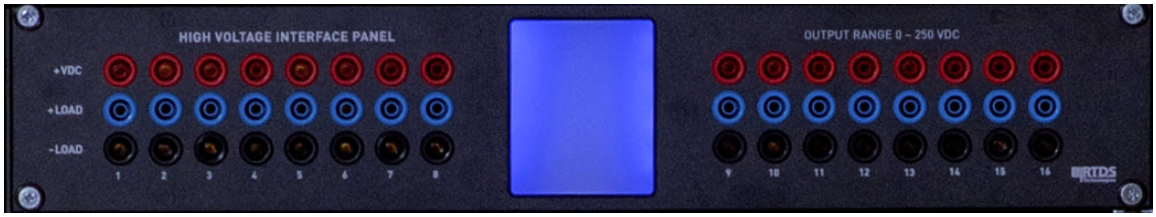
### *4.2.9 Low Voltage Digital Input/Output Interface Panel*

Rack mounted panel, located in the front of a simulator cubicle, used for easy access to the digital input and output (TTL level) from the GTFPI card. The digital inputs are normally high (5V) which is ideal for the easy connection of potential free (dry) contact outputs from conventional protection equipment.




### *4.2.10 250 Vdc Digital Output Interface Panel*

Rack mounted panel, typically located in the front of a simulator cubicle, used to provide dry contacts, controlled by the GTFPI digital output port (TTL level), capable of switching up to 250 Vdc (i.e. station voltage) for breaker status signals, etc.




### 4.3 OPERATING ENVIRONMENT

It is the customer's responsibility to provide an operating environment for the RTDS Simulator where the ambient temperature is maintained between 15 and 30 °C and the relative humidity is between 40% and 90% non-condensing. Additionally, the RTDS Simulator must be housed in a relatively clean environment as would be typical of an office environment.

Each NovaCor chassis consumes a maximum input power of 450 W. The power supplies are designed to operate using a 1-phase voltage in the range of 90 Vrms to 264 Vrms and a frequency range of 47 Hz to 63 Hz.

With the purchase of an RTDS Simulator, RSCAD can be installed on any number of customer computers. The minimum personal computer requirements are:

- Windows 7, 8, or 10 with 4 GB RAM and 3 GHz processor

Please contact us about additional computer recommendations.

## 5 RTDS SIMULATOR SOFTWARE - RSCAD™

In general terms, the RSCAD software falls into one of three distinct categories:

I. Graphical User Interface (GUI)
II. Compiler
III. Power and Control System Component Models

### 5.1 GRAPHICAL USER INTERFACE

All interactions between the user and the RTDS Simulator are performed using a sophisticated, graphically-driven user interface called RSCAD. The RSCAD software can be installed on a standard Windows PC and represents a family of software tools consisting of individual modules used to accomplish various tasks in the overall operation of the Simulator. The most frequently used modules of RSCAD are FILEMANAGER, DRAFT and RUNTIME which are described in further detail below.

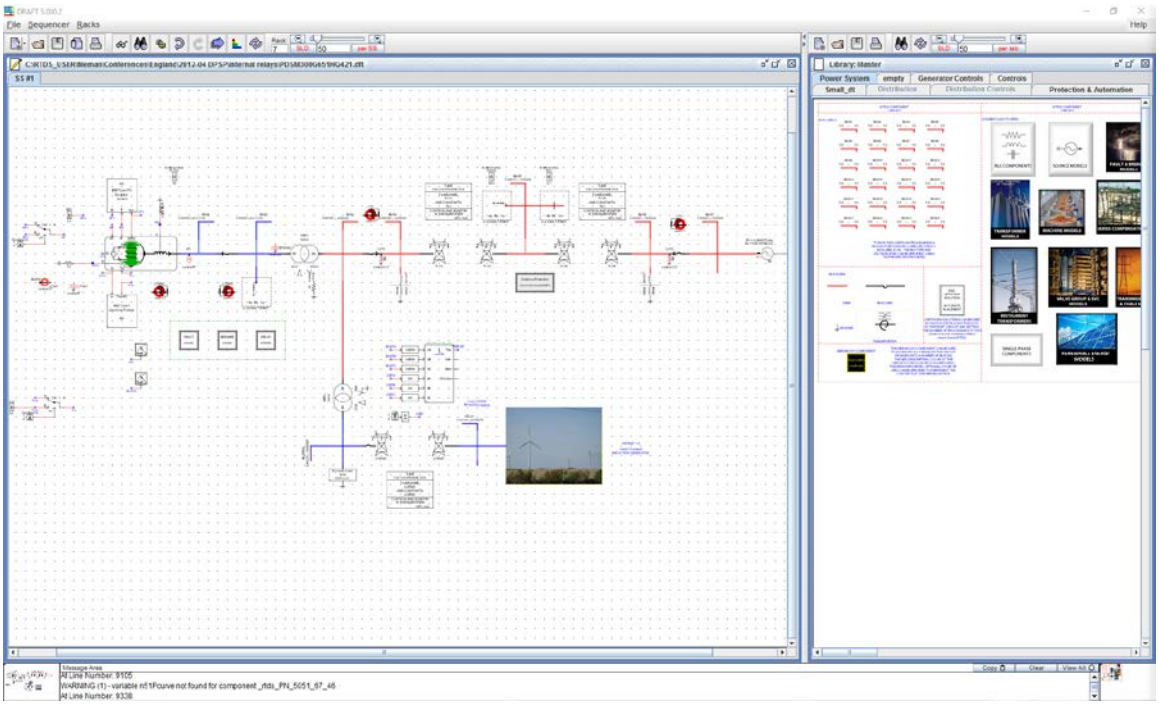
*FILEMANAGER*

The FILEMANAGER module represents the top level of RSCAD through which the graphically driven system is managed. This icon-based file management system aids in organizing a large number of studies and the many files associated with them. Additionally,

it provides a convenient means of exchanging information between users. All other RSCAD modules are invoked from within FILEMANAGER.

*DRAFT*

DRAFT is a pre-processing module used to assemble a simulation circuit and enter its associated parameters. The user simply needs to draw a picture of the circuit. Icons representing individual power system components and control function blocks are arranged on one side of the screen, in the form of a pre-defined or user-defined library. The circuit to be studied is assembled on the other side of the screen. Assembly is accomplished by choosing and copying library components, dragging them to the circuit assembly area, and interconnecting them in an appropriate manner. Actions are mouse and/or keyboard driven for minimal effort and maximum speed. Once the circuit assembly and data entry is complete, the user can save and compile the circuit for simulation.



*RSCAD DRAFT*

The power system circuit can be viewed in either 3-phase or Single Line Diagram (SLD) format. DRAFT also has the ability to include hierarchy areas so that circuit details can be hidden from view in higher levels.

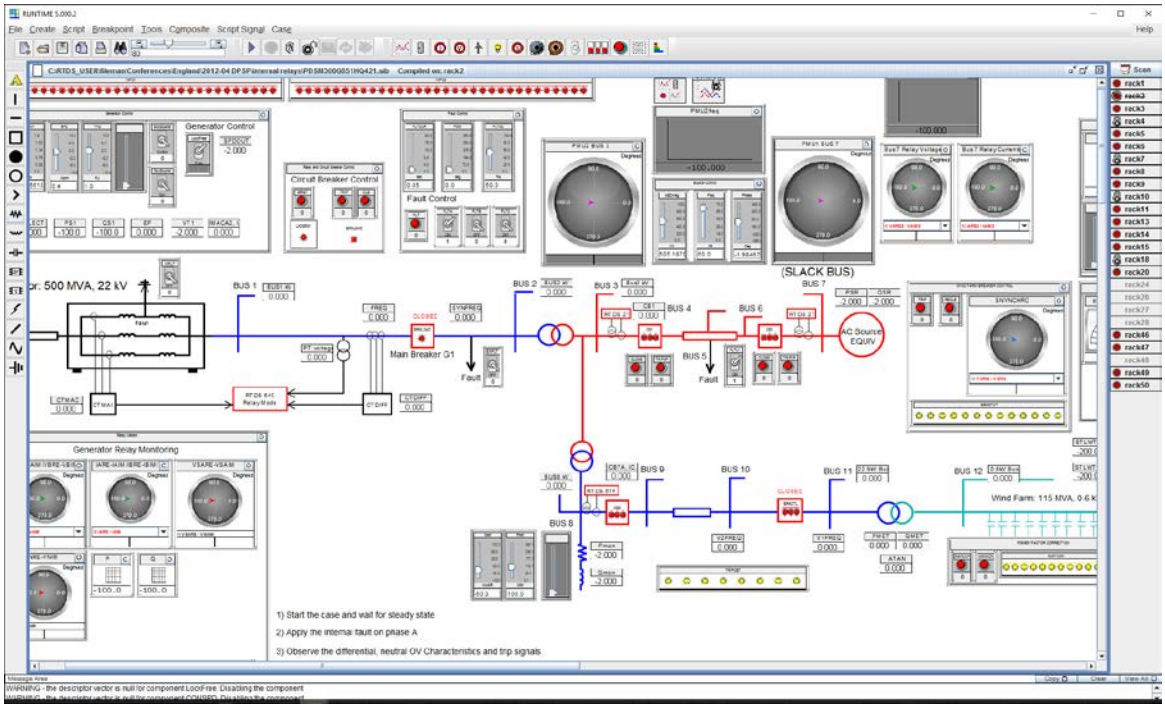
*RUNTIME*

Operation and control of the RTDS Simulator hardware is accomplished using the RUNTIME module. RUNTIME allows one or more operator consoles to be created, through which individual simulation cases can be downloaded and controlled. During the simulation, the user can monitor specified system quantities using graphical icons of

meters, plots, vector displays, etc. In addition, it is also possible to dynamically interact with the simulation as it runs by creating push buttons, set-point sliders, switches, etc. As an example, a fault can be applied at a pre-defined point in the power system by pushing a button on the screen.

A detailed examination of fast changing (transient) signals is accomplished using the plot facilities available in RUNTIME. Plots are updated only at the request of the operator or upon the occurrence of an operator-initiated transient (e.g. application of a fault from RUNTIME). The signals displayed on a plot are captured in real time by the NovaCor and stored in local memory until the specified capture interval has elapsed. Once the entire event has been stored, the data is transferred from the NovaCor to the appropriate plot component on the workstation screen. Data captured and displayed using the RUNTIME plot can also be saved to the hard-drive of the host workstation for further analysis.

RUNTIME is also used to analyze and evaluate captured waveforms as well as prepare output plots in a report-ready format. The plotting features available include calculator and other useful functions that can be applied to the captured waveforms.




*RSCAD RUNTIME*

*AUTOMATED SIMULATOR OPERATION*

A facility is provided within RSCAD to allow automated simulator operation (also known as batch mode operation or scripting). In many situations, particularly when testing protective relays, a large number of similar simulation cases must be run and evaluated (e.g. point on wave switching, varying fault type and fault impedance, etc.). In such

situations, an automated or batch operating mode that minimizes the required user interaction is essential.

The automated simulator operation software can be divided into three major components:

- Record and replay facility
- Script file facility
- Compiling pre-processor facility

The record and replay feature is invoked through the RUNTIME module and allows the user to record manually initiated events such as starting cases, adjusting system set points, applying faults, storage of output waveforms, etc. Once a series of actions has been recorded, it can be replayed many times without the need for further interaction by the user.

The script file feature is essentially an extension of the record and replay facility through which the user can manually introduce additional functions or events to pre-recorded operations. When the record feature, described above, is used, a "C-like" script text file is automatically generated and saved. After recording, the script file may also be modified to introduce refinements or to create a more complex script sequence. For example, the user may introduce result analysis functions such as FFTs, max/min searches, logical operations, etc. The results of these functions can then be displayed either graphically, stored in separately defined output files, or printed. Conditional/adaptive looping via if, for, and while statements may also be added to the script file.

The RTDS pre-processing compiler provides a method of automatically re-compiling simulation cases when certain types of circuit variables are changed. Since pre-processor variables can only be changed when the simulation is stopped, the re-compile is initiated when the command is given to start the case. As in the case of record/replay and script file management, all operations relating to the pre-processor are accomplished through RUNTIME. Modification of a fault impedance value represents a typical situation in which the pre-processor can be applied. In this case, the user may specify in RUNTIME or within a script file that the fault impedance at a particular point in the circuit should change from one value to another. The next time the simulation case is started, the new value of the fault impedance will be applied.

Since the principal goal of the batch operating mode is to reduce user interaction and facilitate studies which require large numbers of cases, record/replay, the script file facility and pre-processor variables are normally used together to suit the particular study at hand.

## 5.2 COMPILER

An important link between the graphical user interface software and code that runs on the RTDS Simulator hardware is a specially designed compiling system. The RSCAD compiler takes the circuit layout and parameters from DRAFT and produces the parallel processing code required by the processors. In addition, the compiler assigns the role that each core will play during the simulation based on the required circuit layout and the hardware available. The assignment of components to specific cores can be done automatically or manually (user defined). Manual assignment of cores can be important for assigning I/O interface points which should remain constant throughout a project.

In addition to producing the processor code, the compiler also produces a user-readable file indicating the function of each core in the particular case being considered. This so-called MAP File also directs the user to I/O points available for a particular simulation case.

## 5.3 POWER AND CONTROL SYSTEM COMPONENT MODELS

In order to produce the code to run on the NovaCor, the RSCAD compiler accesses a library of pre-defined power and control system components. Since the length of these software models directly impacts the minimum achievable simulation timestep (i.e. if the executable code is short then the timestep will be short), great care has been given to create efficient code. The user is **never required** to write, edit or even access the component model code. The models are simply stored in the libraries for use by the compiler.

Another important point with respect to the creation of new models is that the user can introduce new power and control system components (written in C) for use with the RTDS Simulator via the Component Builder module described below.

### POWER SYSTEM COMPONENT LIBRARY

RSCAD contains a comprehensive library of power system components which has been growing and enhanced for more than 20 years. Some of the main components included in the RSCAD power system library are:

- Standard Timestep Components
  - Multi-phase (max. 12 cond.), coupled travelling wave transmission lines
  - Transformers (2 or 3 winding) with saturation and hysteresis
  - Synchronous machines with Multi-Mass modelling and internal faults
  - Asynchronous (induction) machines
  - Voltage sources with definable equivalent impedances, source magnitude, frequency and phase
  - Passive Resistive, Inductive and Capacitive components
  - Non-linear Inductor
  - Circuit breakers & fault switched
  - Series capacitors with ZnO arrestors and bypass switches

- Thyristor Controlled Series Capacitors (TCSC)
- HVDC valve groups (transmission and back-to-back) – 6 and 12 pulse
- Switched filter bank model
- Bus Arrester
- Static VAR Compensators
- Instrument transformers including current transformers (CT), inductive voltage transformers (PT), capacitive voltage transformers (CVT)
- COMTRADE Playback

- Small Timestep Components
  - Switching devices
    - ❖ Breakers
    - ❖ Diodes
    - ❖ Thyristors
    - ❖ IGBT – diode pairs
  - Modular Multilevel Converter (MMC valves)
  - 2- and 3-level bridges
  - High accuracy signal generators
  - Machines (induction, synchronous, PMSM)
  - Traveling wave and pi-section transmission lines and cables
  - Passive components and filters
  - Transformers (2 & 3 winding)

**CONTROL SYSTEM COMPONENT LIBRARY**

The following are just some of the function blocks included in the RSCAD control system library:

| | |
|---|---|
| 3 Phase - 2 Phase Conversion | Analogue - Digital Conversion |
| Compare | Constant Input |
| Dead Band | Delay (Sampled) |
| Differential Pole | Digital - Analogue Conversion |
| Digital Input | Digital Output |
| Dual Port Memory Read | Export |
| Dynamic Limits | Full Wave Rectifier |
| Floating Point - Integer Conversion | Integer Constant |
| Gain | Integer - Floating Point Conversion |
| Import | 1st Order Lag |
| Integrator | Limits |
| Lead-Lag | Logic gates |
| Log, Ln, 10X, eX | Monostable |
| ABS, 1/X, Sqrt(X), X2 | Non-Linear Gain |
| Multiplier | Push Button Input |
| NOT | Ring Counter |
| PI-Regulator | Selector |

| | |
|---|---|
| Sample & Hold | Signal Switch |
| Signal Generator | Subsystem Assignment |
| Slider Input | Switch Input |
| Summing Junction | Trig. ArcTan(X,Y) |
| Timer | Trig. sin-1(X), cos-1(X) |

**COMPONENT BUILDER**

Component Builder provides an interface for users to create new components that can be included in real time simulations. The graphics and data entry menus for DRAFT components are created using drawing facilities and GUI input respectively. In addition, Component Builder allows the real time code for the component to be created in C. The machine code for the RTDS Simulator is generated from the C code by the Component Builder compiler. Most of the models found in RSCAD have been developed in Component Builder.

**SMALL TIMESTEP SUBNETWORKS**

A technique is available to allow subnetworks to be represented with a timestep of less than 1.5 µs. With such a small timestep, high frequency PWM firing pulse controllers can be accurately tested. The technique allows the user to configure multi-level bridges with a maximum of 36 switching elements (IGBT – diode pairs are considered one element) and 30 single phase nodes. This allows Voltage Source Converter (VSC)-based HVDC, FACTS, renewable energy devices, etc. to be modelled within a small timestep subnetwork.

VSCs with PWM switching cannot be properly represented in the standard timestep because the switches may change state multiple times during 50 µs. In off-line simulation programs, the fast switching of the VSCs can be taken into account by reducing the timestep to the 10 µs range and by using interpolation. However, because interpolation requires the simulation to stop and back up in time, it is not suitable for real time simulation where a continuous hard real time solution must be maintained. By reducing the timestep to the 1-3 µs range, the small timestep subnetworks can allow each switching component to change state every timestep without the use of interpolation.

A new technique is now available to run some fixed topology bridges (2/3 level) at a sub small timestep. Up to 5 sub steps can be included in 1 small timestep, meaning switching losses are reduced by ~50% and PWM switching frequencies of up to 40 kHz can be applied to a 2 level bridge.

The small timestep subnetworks can be connected to the main simulation running with a typical timestep of 30-50 µs. This allows an accurate and comprehensive power system to be represented together with the detail and high fidelity of the small timestep model.

The small timestep subnetworks are connected to the main simulation via a numerical interface. Typically, the interface is made using transmission lines or at converter transformers or series reactors.

Multiple small timestep subnetworks can be connected to one another via traveling wave models. The method is similar to subsystem splitting techniques for standard timestep simulations and allow the subnetwork to be expanded.

Many different types of VSC-based schemes have been created using the small timestep subnetworks, such as:

- MMC-based FACTS and HVDC
- DFIG and full converter-based wind generators
- 2- and 3-level converters for renewables and energy storage
- 2- and 3-level converter-based FACTS and HVDC

# APPENDIX 1
# SYSTEM HARDWARE ALLOCATION EXAMPLES

**General Comments**

1. Each NovaCor chassis has one processor with 10 cores. Each core has 300 load units.

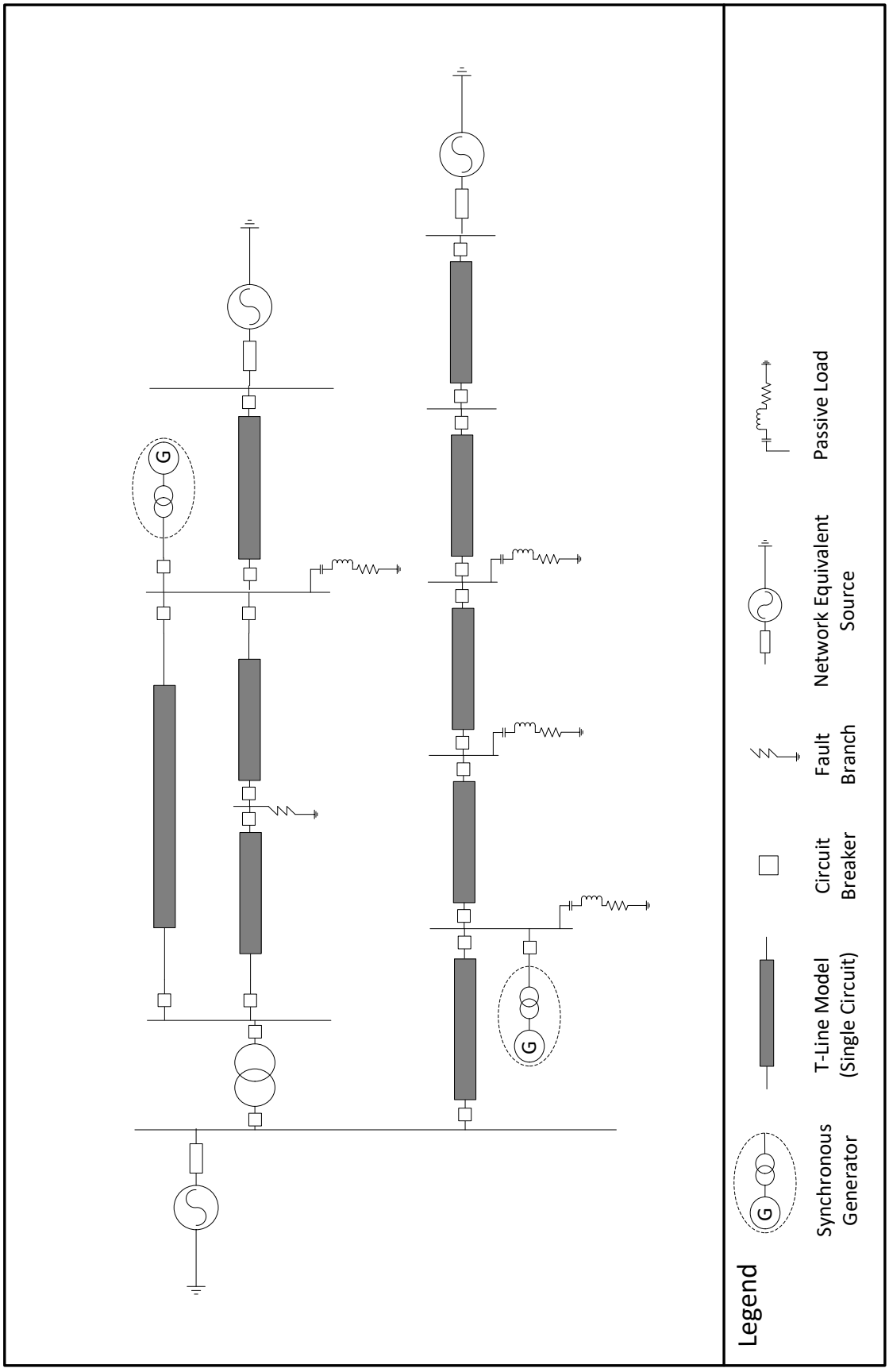
2. NovaCor can run an entire regular timestep network on a single core (network solution, control, and power system components). For systems containing 90 or fewer single-phase nodes, 180 load units are available on the network solution core for power system components (lines, machines, transformers, etc.).

3. Controls components can be stacked on either network solution or power system cores, or use their own dedicated core.

4. For simulations with greater than 90 single-phase nodes, the network solution requires a full core and up to 300 single-phase nodes can be solved per network solution. Two network solutions are allowed per chassis which provide maximum of 600 single-phase nodes split into at least two subsystems (using travelling wave splitting techniques).

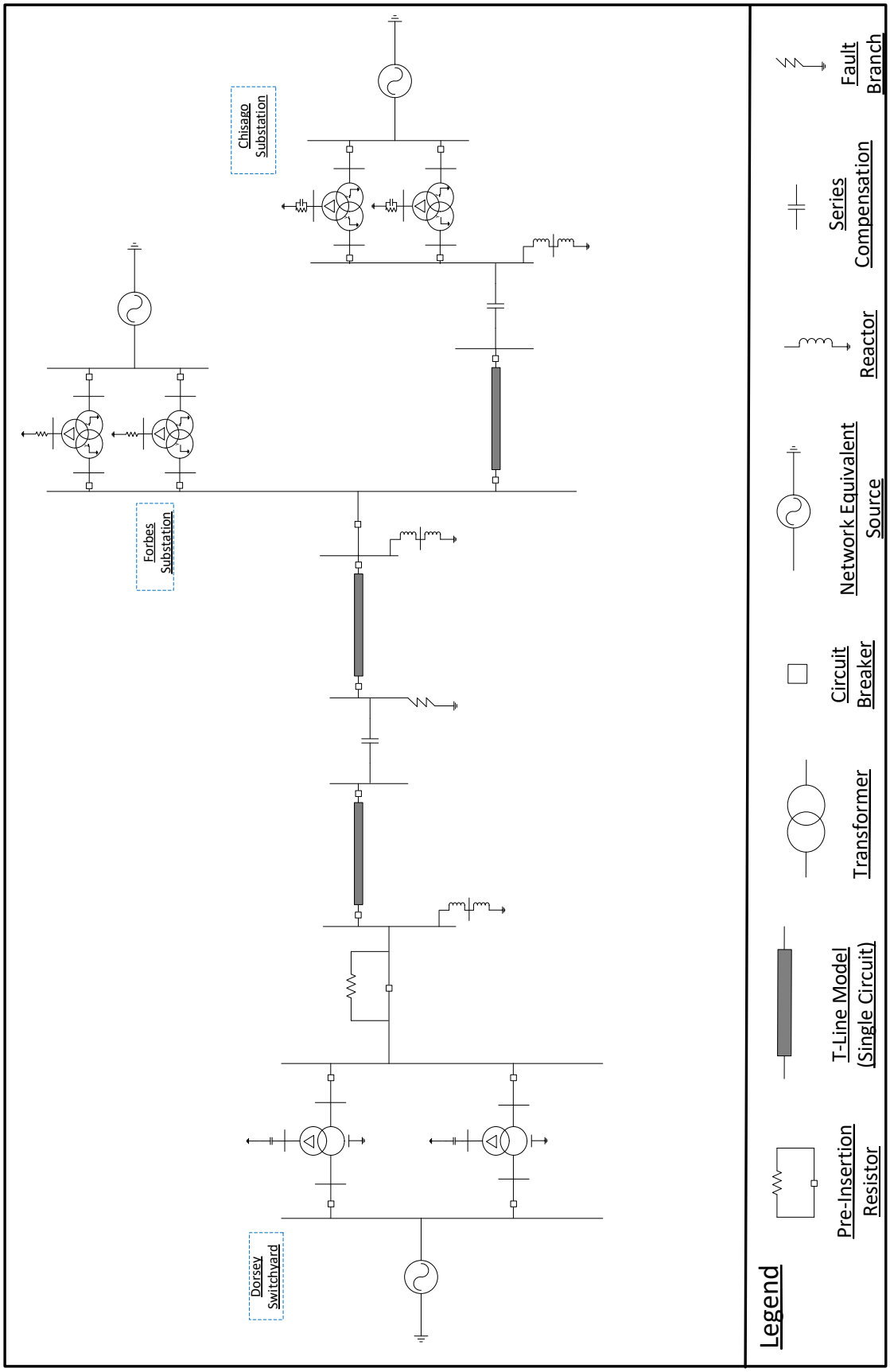
5. Up to 300 load units are available on each of the non-network solutions cores for power system components (lines, machines, transformers, etc.).

6. Passive components (i.e. shunt reactors) are solved by the network solution and do not require additional cores.



# 10 Bus System - Core allocation

| Component | Qty | # of NovaCor Load Units | Comments |
|---|---|---|---|
| Nodes (1Ø) and controls | (102-72*) = 30 | 120 units | 1 network solution / 1 subsystem<br>*72 embedded t-line, transformer, and generator nodes not solved by the network solution.<br>Generator, breaker, and fault control plus digital input and output signals |
| Single Circuit Lines (3Ø) | 9 | 90 units | Traveling wave, Bergeron type model, with embedded breakers |
| Generator / Transformer (3Ø) | 2 | 40 units | Integrated generator / transformer model (intermediate nodes not counted in Network Solution) |
| Transformer (3Ø) | 1 | 15 units | 3Ø Transformer with Saturation and embedded breakers |
| Source (3Ø) | 3 | 30 units | |
| **Total No.**<br>**Core Units** | | **295 units** | **300 units/core x 10 cores/chassis** |
| **Total No.**<br>**Cores** | | **1**<br>**Core** | **One (1) chassis requiring a minimum of:**<br>**One (1) Core** |

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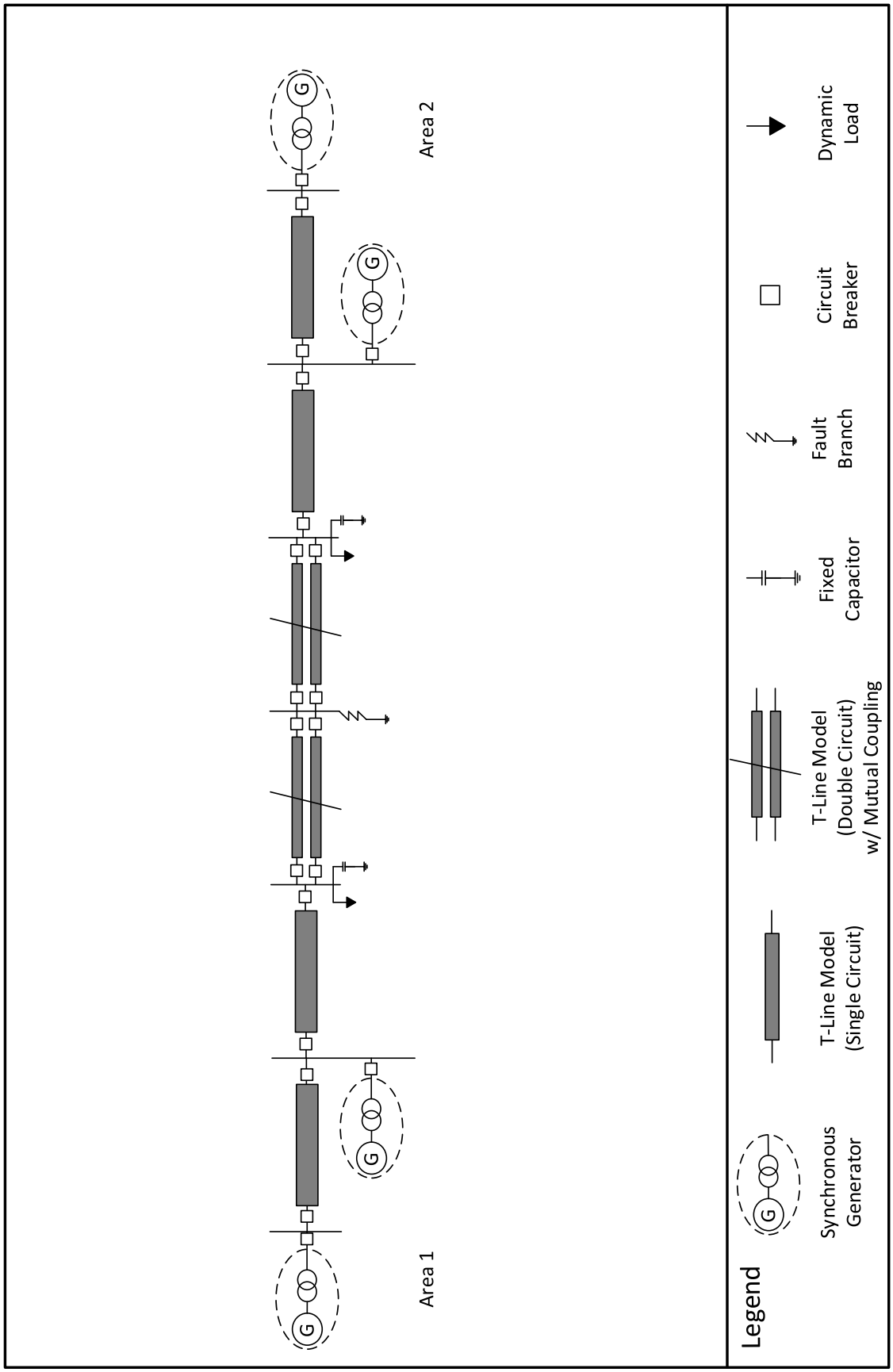
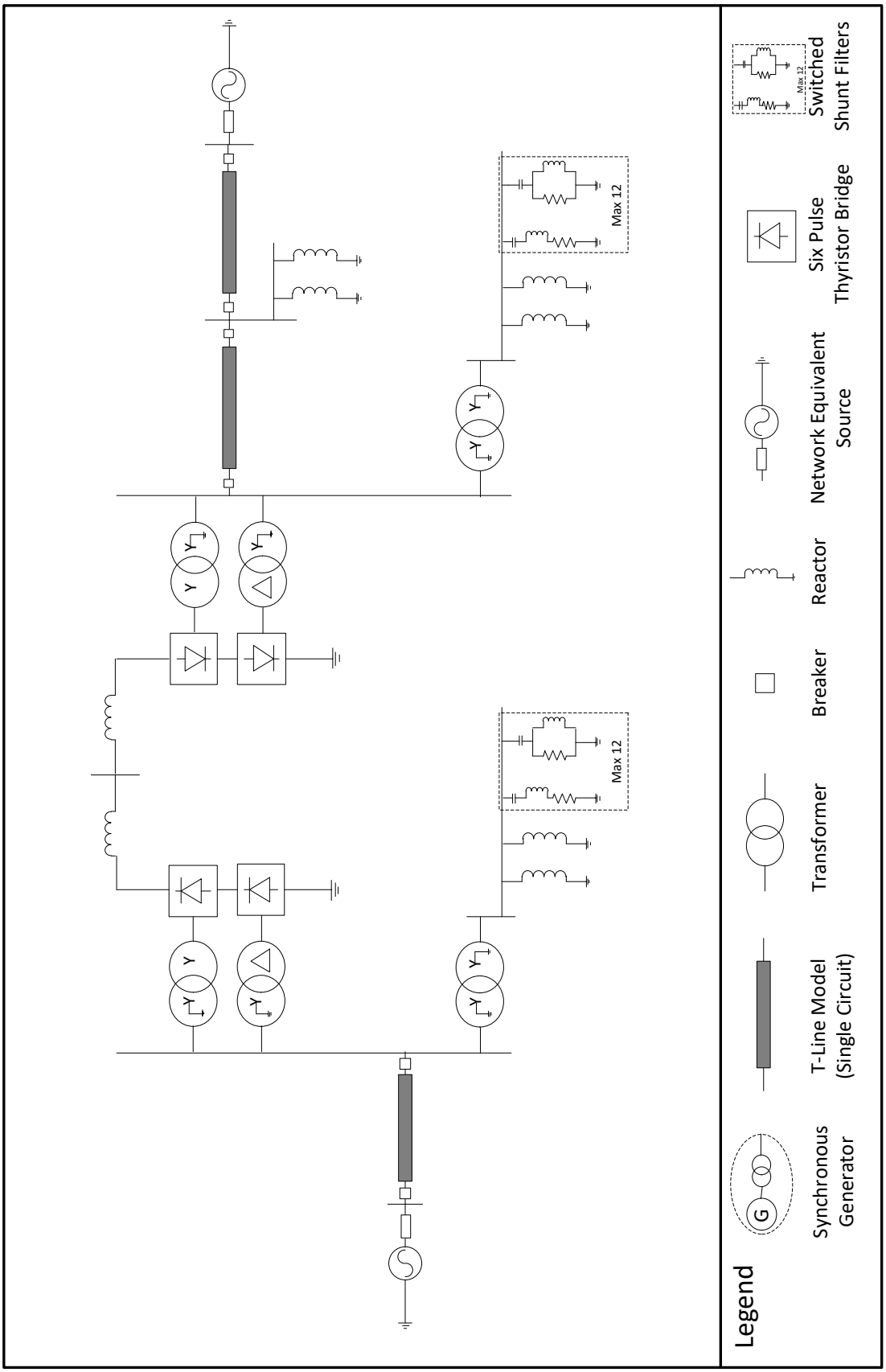
# Dorsey-Forbes-Chisago Case - Core allocation

| Component | Qty | # of NovaCor Load Units | Comments |
|---|---|---|---|
| Nodes (1Ø) and controls | (105-18*) = 87 | 120 units | 1 network solution / 1 subsystem<br>*18 embedded t-line nodes not solved by the network solution.<br>Generator, breaker, and fault control plus digital input and output signals |
| Single Circuit Lines (3Ø) | 3 | 30 units | Traveling wave, Bergeron type model, with embedded breakers |
| Transformer (3Ø) | 4 | 60 units | 3Ø Transformer with Saturation and external connection |
| Auto-Transformer (3Ø) | 2 | 20 units | 3Ø Auto-Transformer with Saturation |
| Switched cap | 2 | 40 units | |
| Source (3Ø) | 3 | 30 units | |
| **Total No.<br>Core Units** | | **300 units** | **300 units/core x 10 cores/chassis** |
| **Total No.<br>Cores** | | **1<br>Core** | **One (1) chassis requiring a minimum of:<br>One (1) Core** |



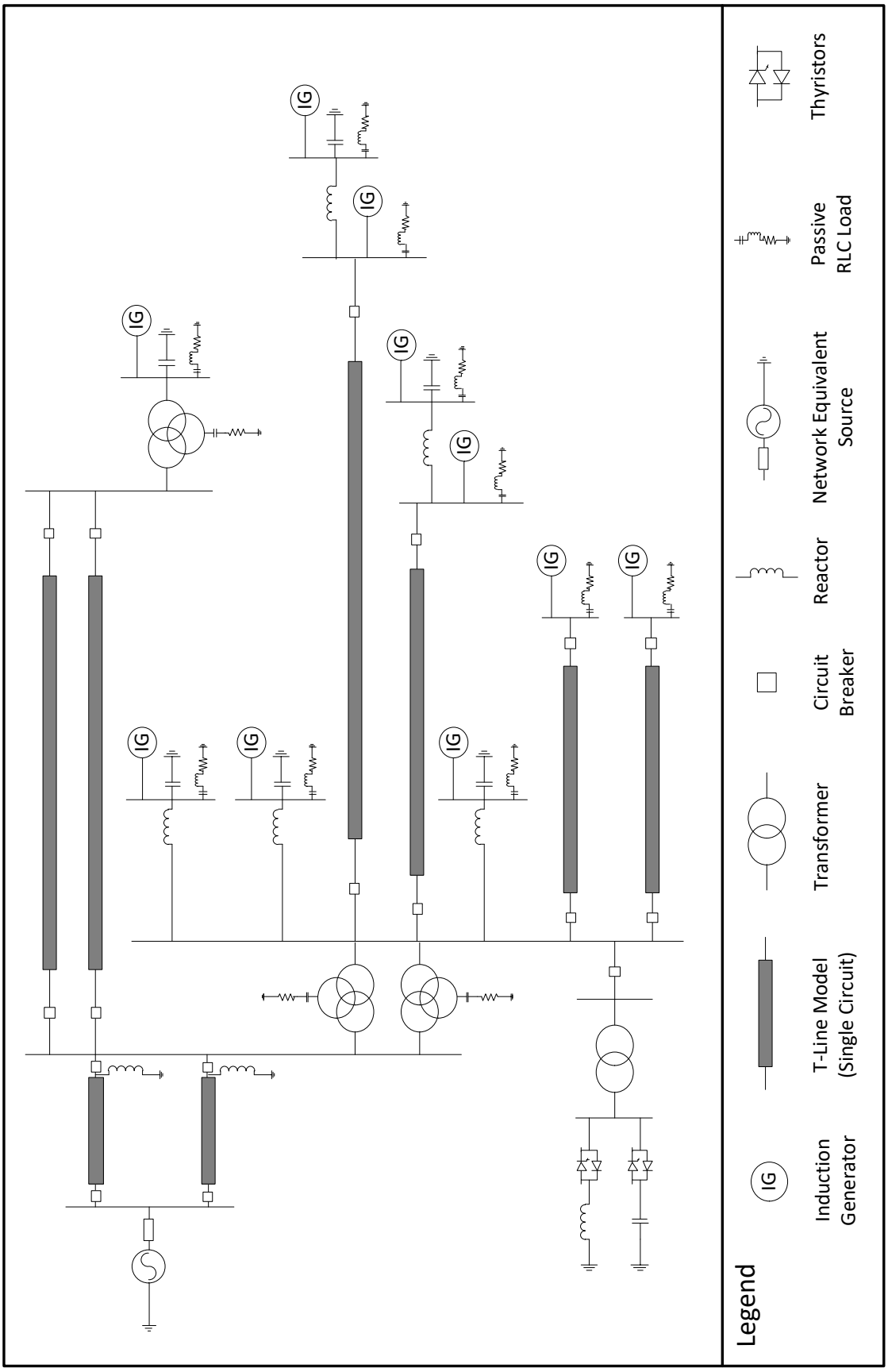
# Kundur's Two Area Power System - Core allocation

| Component | Qty | # of NovaCor Load Units | Comments |
|---|---|---|---|
| Nodes (1Ø) and controls | (81-60*) = 21 | 120 units | 1 network solution / 1 subsystem<br>*60 embedded generator, t-line nodes not solved by the network solution. |
| Single Circuit Lines (3Ø) | 4 | 40 units | Traveling wave, Bergeron type model, with embedded breakers |
| Double Circuit Lines (3Ø) | 2 | 60 units | Traveling wave, Bergeron type model, with embedded breakers |
| Generator / Transformer (3Ø) | 4 | 80 units | Integrated generator / transformer model (intermediate nodes not counted in Network Solution) with embedded breaker |
| Dynamic Load (3Ø) | 2 | 20 units | |
| **Total No.**<br><br>**Core Units** | | **320 units** | **300 units/core x 10 cores/chassis** |
| **Total No.**<br><br>**Cores** | | **2**<br><br>**Cores** | **One (1) chassis requiring a minimum of:**<br><br>**Two (2) Cores** |



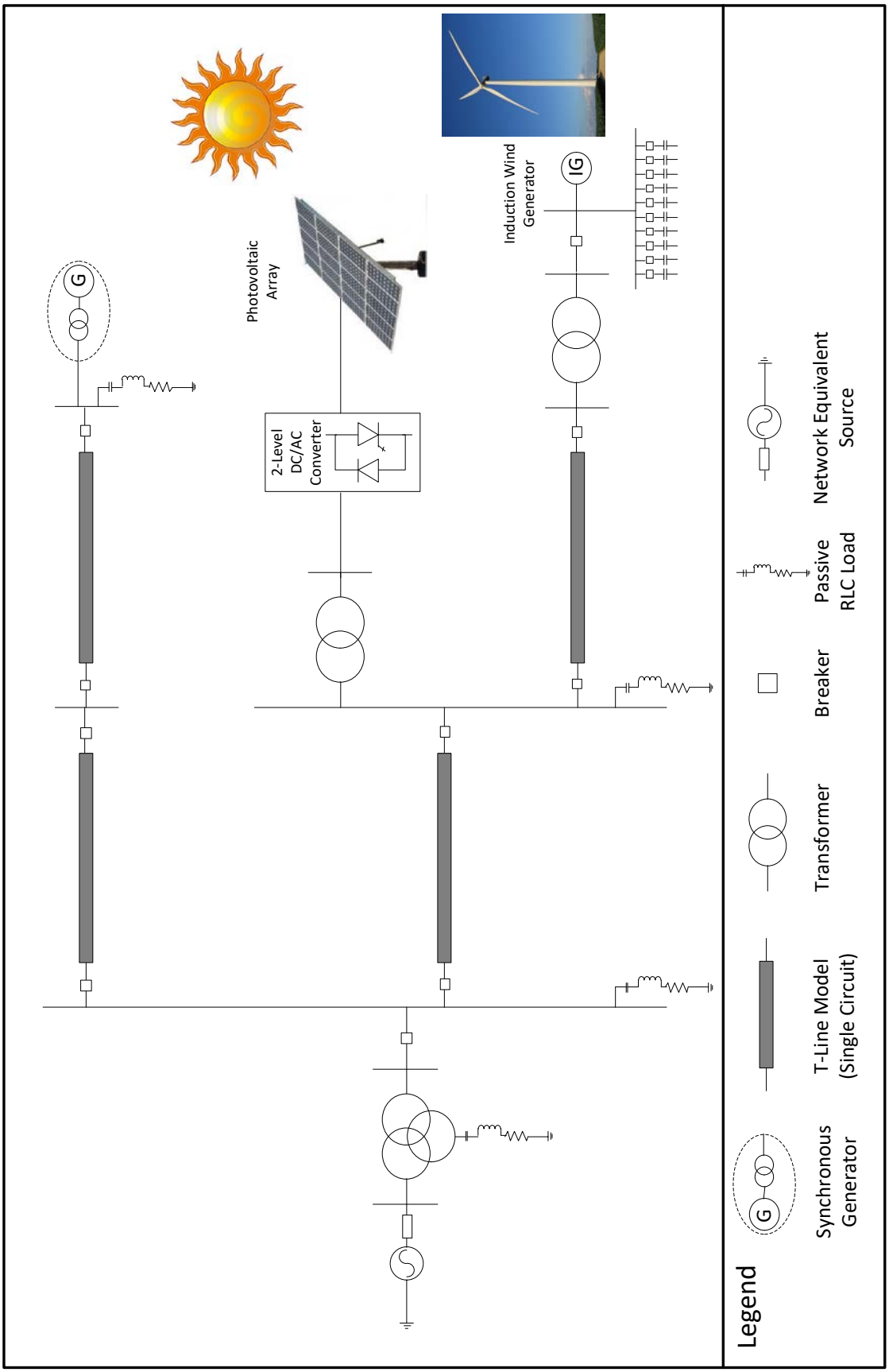
# HVDC – Core allocation

| Component | Quantity | # of NovaCor Load Units | Comments |
|---|---|---|---|
| Nodes (1Ø) and controls | (54-30*) = 24 | 120 units | 1 network solution / 1 subsystem<br>*30 embedded t-line, transformer, and generator nodes not solved by the network solution<br>Generator, breaker, and fault control plus digital input and output signals |
| Six Pulse Valve Group | 4 | 80 units | |
| Switched Shunt Comp (3Ø) | 2 | 60 units | |
| Single Circuit Lines (3Ø) | 3 | 30 units | Traveling wave, Bergeron type model, with embedded breakers |
| Transformer (3Ø) | 2 | 30 units | 3Ø Transformer with Saturation and embedded breakers |
| Source (3Ø) | 2 | 20 units | |
| **Total No. Core Units** | | **340 units** | **300 units/core x 10 cores/chassis** |
| **Total No. Cores** | | **2 Cores** | **One (1) chassis requiring a minimum of:**<br>**Two (2) Cores** |



# 16-Bus System – Core allocation

| Component | Quantity | # of NovaCor Load Units | Comments |
|---|---|---|---|
| Nodes (1Ø) and controls | (153-105*) = 48 | 120 units | 1 network solution / 1 subsystem<br>*105 embedded t-line, transformer, and generator nodes not solved by the network solution<br>Generator, breaker, and fault control plus digital input and output signals |
| SVC | 2 | 40 units | |
| Induction Motor | 10 | 100 units | Includes embedded breaker. |
| Single Circuit Lines (3Ø) | 8 | 80 units | Traveling wave, Bergeron type model, with embedded breakers |
| Transformer (3Ø) | 4 | 60 units | 3Ø Transformer with saturation and embedded breakers |
| Source (3Ø) | 2 | 20 units | |
| **Total No.**<br>**Core Units** | | **420 units** | **300 units/core x 10 cores/chassis** |
| **Total No.**<br>**Cores** | | **2**<br>**Cores** | **One (1) chassis requiring a minimum of:**<br>**Two (2) Cores** |

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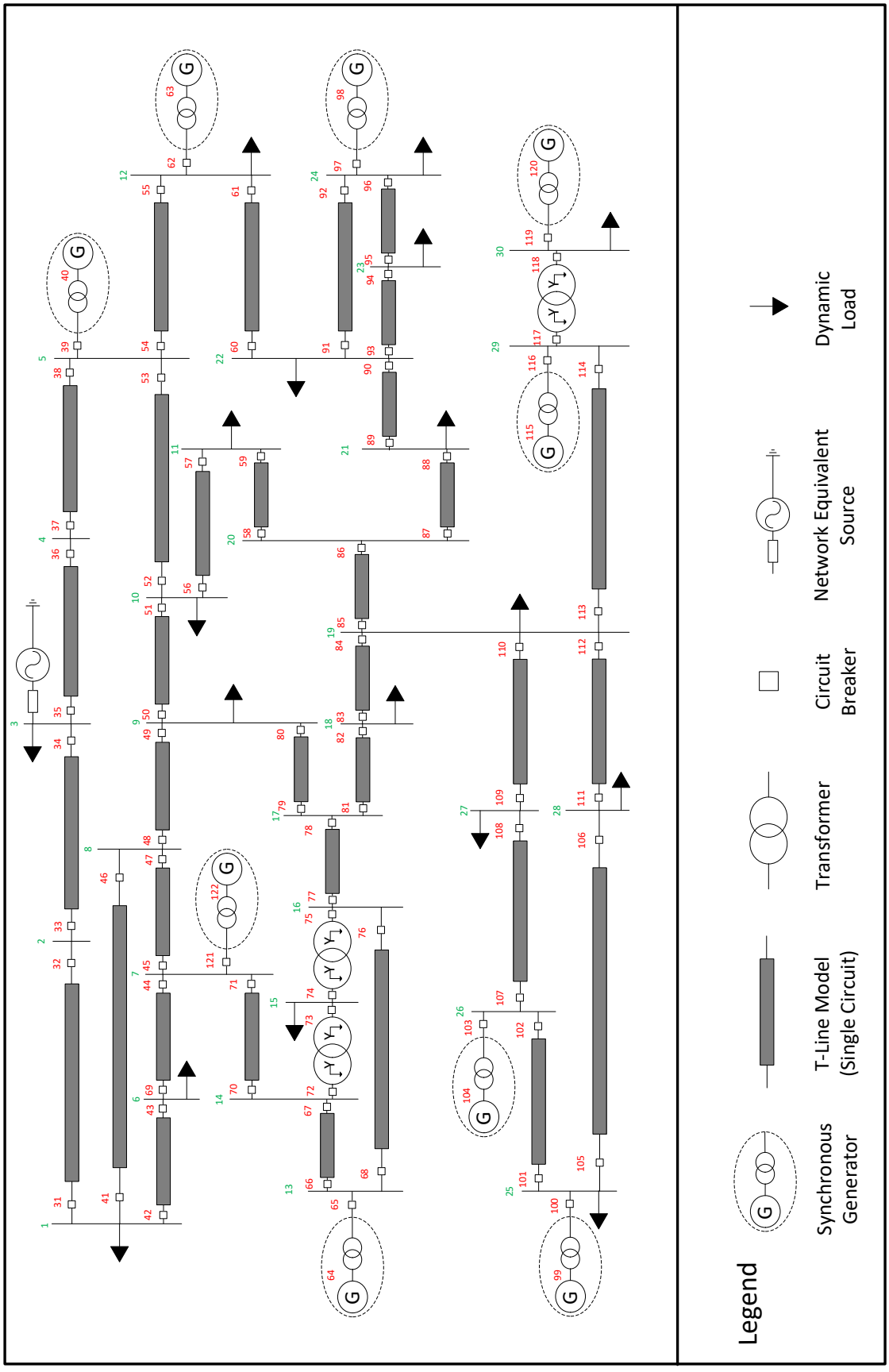
# Distributed Generation – Core allocation

| Component | Quantity | # of NovaCor Load Units | Comments |
|---|---|---|---|
| Nodes (1Ø) and controls | (81-51*) = 30 | 120 units | 1 network solution/1 subsystem<br>*51 embedded t-line, transformer, and generator nodes not solved by the network solution<br>Generator, wind turbine, breaker, and fault control |
| Single Circuit Lines (3Ø) | 4 | 40 units | Traveling wave, Bergeron type model, with embedded breakers |
| Induction Generator | 1 | 10 units | Includes embedded breaker |
| Generator / Transformer (3Ø) | 1 | 20 units | Integrated generator – transformer model (intermediate nodes not counted) |
| Photovoltaic Array | 1 | 10 units | |
| Transformer (3Ø) | 3 | 45 units | 3Ø Transformer with Saturation and embedded breakers |
| Switched cap | 10 | 100 units | |
| Source (3Ø) | 1 | 10 units | |
| Small dT Subnetwork | 1 | 300 units | 2-level VSC-based converter for photovoltaic generator |
| **Total No.**<br>**Core Units** | | **655 units** | **300 units/core x 10 cores/chassis** |
| **Total No.**<br>**Cores** | | **3**<br>**Cores** | **One (1) chassis requiring a minimum of:**<br>**Three (3) Cores** |

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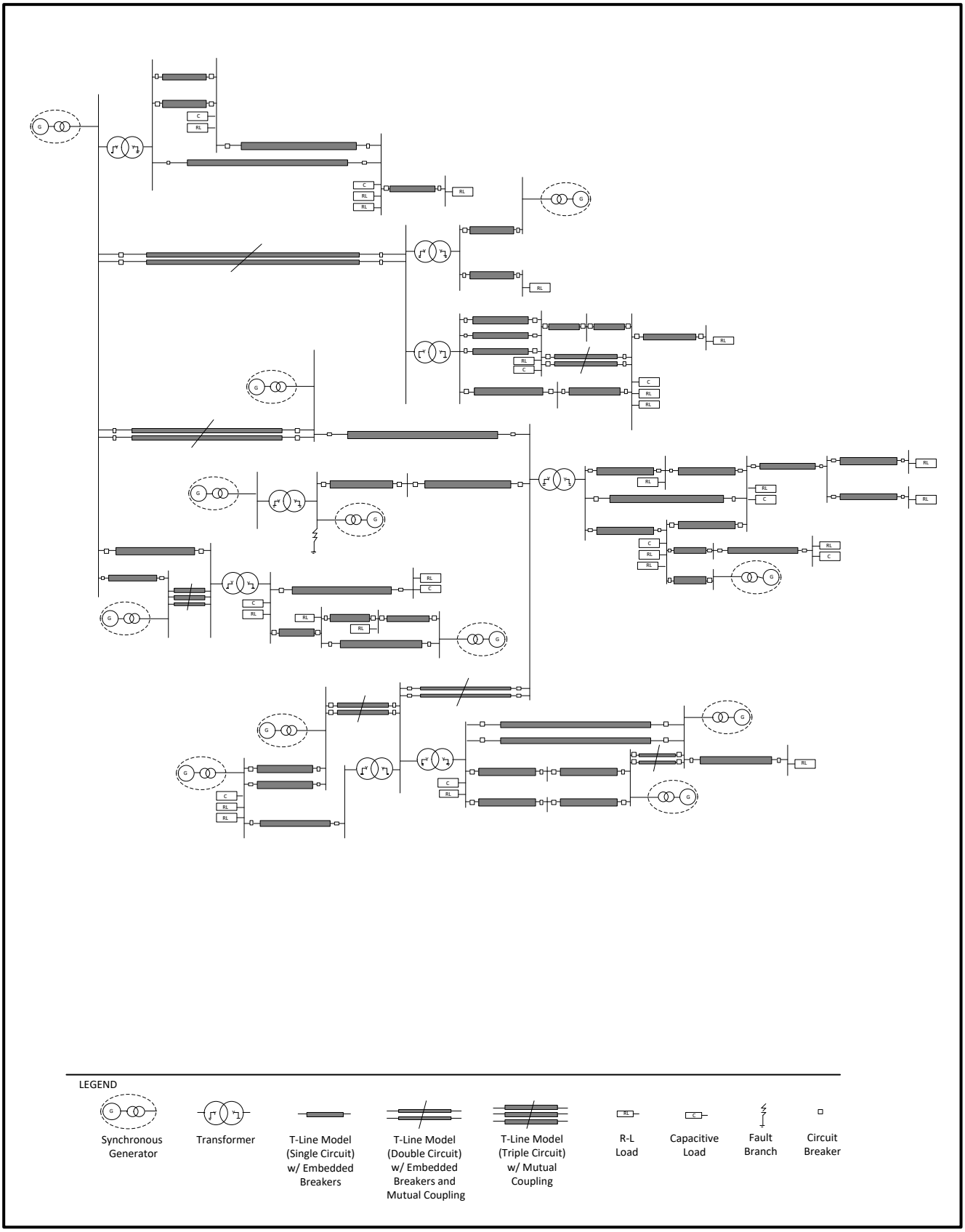
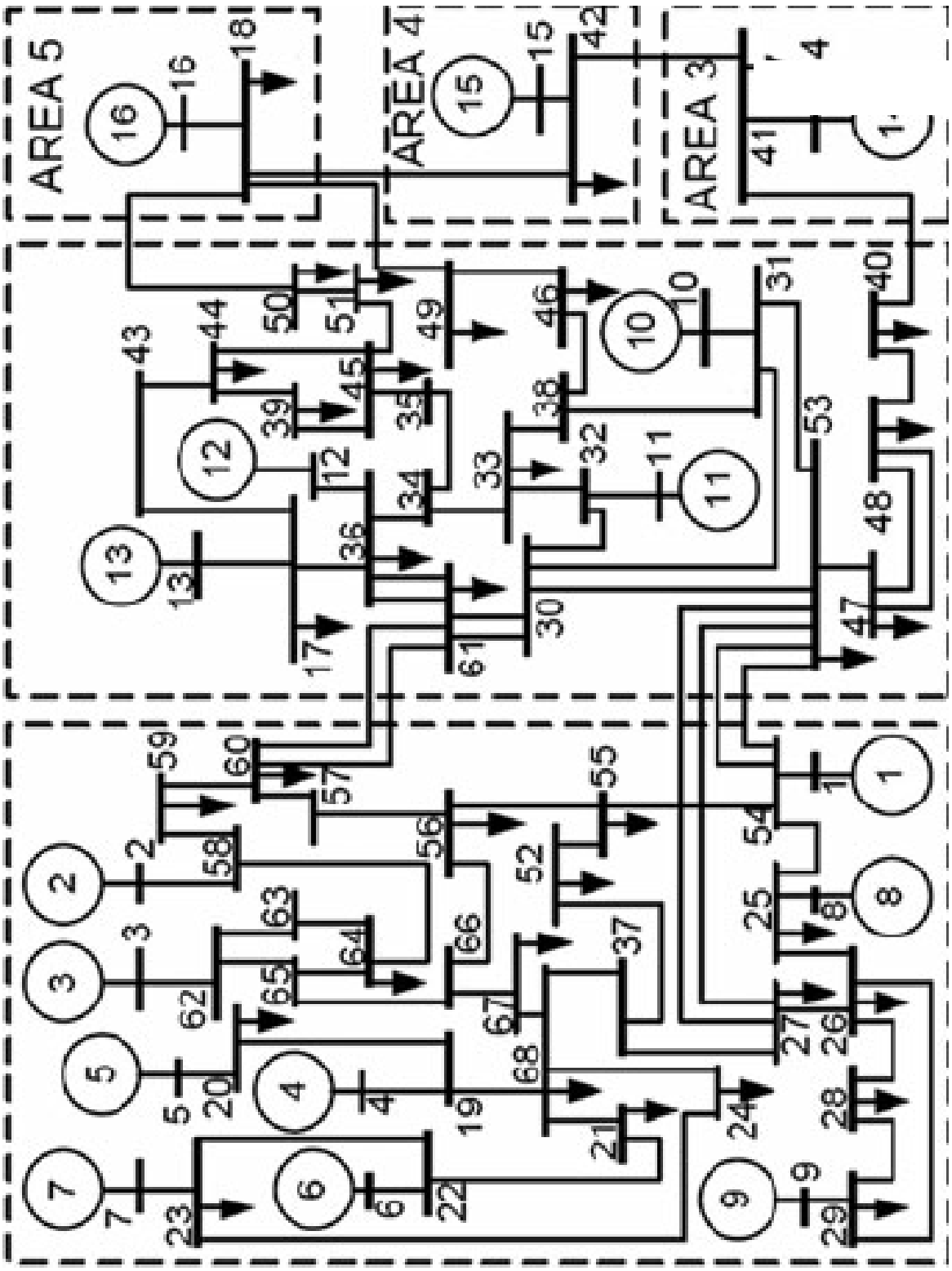
# IEEE 39 Bus System - Core allocation

| Component | Quantity | # of NovaCor Load Units | Comments |
|---|---|---|---|
| Nodes (1Ø) and controls | (366-276*) = 90 | 120 units | 1 network solutions / 1 subsystem<br>*276 embedded t-line, transformer, and generator nodes not solved by the network solution<br>Generator, breaker, and fault control plus digital input and output signals |
| Single Circuit Lines (3Ø) with breakers | 34 | 340 units | Optimized Bergeron model with embedded breakers |
| Generator (3Ø) | 9 | 180 units | Integrated generator – transformer model (intermediate nodes not counted) |
| Transformer (3Ø) | 3 | 45 units | 3Ø Transformer with Saturation and embedded breakers |
| Source (3Ø) | 1 | 10 units | |
| Dynamic Loads | 18 | 180 units | |
| **Total No.<br>Core Units** | | **875 units** | **300 units/core x 10 cores/chassis** |
| **Total No.<br>Cores** | | **3<br>Cores** | **One (1) chassis requiring a minimum of:<br>Three (3) Cores** |



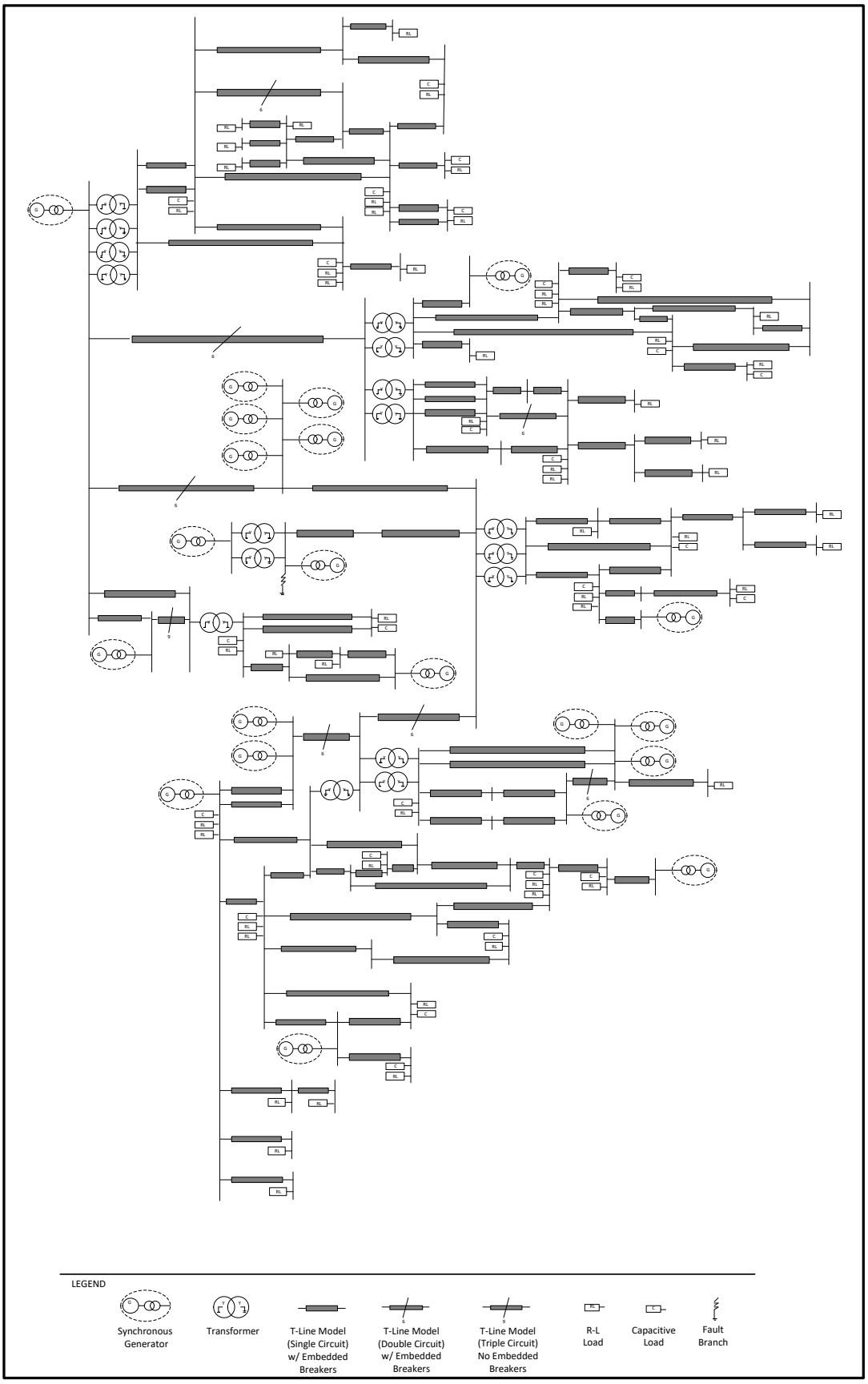
# 59 Bus System - Core Allocation

| Component | Quantity | # of NovaCor Load Units | Comments |
|---|---|---|---|
| Nodes (1Ø) and controls | (645-468*) = 177 | 300 units | 1 network solution / 1 subsystem<br>*468 embedded t-line, transformer, and generator nodes not solved by the network solution<br>Generator, breaker, and fault control plus digital input and output signals |
| Single Circuit Lines (3Ø) | 46 | 460 units | Optimized Bergeron model with embedded breakers |
| Double Circuit Lines (2x3Ø) | 6 | 180 units | Optimized Bergeron model with embedded breakers |
| Triple Circuit Lines (3x3Ø) | 1 | 40 units | Optimized Bergeron model |
| Generator / Transformer (3Ø) | 12 | 240 units | Integrated generator – transformer model (intermediate nodes not counted) |
| Transformer (3Ø) | 8 | 160 units | 3Ø Transformer with Saturation and embedded breakers |
| **Total No.**<br><br>**Core Units** | | **1380 units** | **300 units/core x 10 cores/chassis** |
| **Total No.**<br><br>**Cores** | | **5**<br><br>**Cores** | **One (1) chassis requiring a minimum of:**<br><br>**Five (5) Cores** |



# IEEE 68 Bus System - Core Allocation

| Component | Quantity | # of NovaCor Load Units | Comments |
|---|---|---|---|
| Nodes (1Ø) and controls | (600-450*) = 150 | 300 units | 1 network solution / 1 subsystem<br>*450 embedded t-line, transformer, and generator nodes not solved by the network solution<br>Generator, breaker, and fault control plus digital input and output signals |
| Single Circuit Lines (3Ø) | 55 | 550 units | Optimized Bergeron model with embedded breakers |
| Double Circuit Lines (2x3Ø) | 3 | 90 units | Optimized Bergeron model with embedded breakers |
| Generator / Transformer (3Ø) | 16 | 320 units | Integrated generator – transformer model (intermediate nodes not counted) |
| Transformer (3Ø) | 4 | 60 units | 3Ø Transformer with Saturation and embedded breakers |
| Dynamic Loads | 35 | 350 units | |
| **Total No. Core Units** | | **1670 units** | **300 units/core x 10 cores/chassis** |
| **Total No. Cores** | | **6 Cores** | **One (1) chassis requiring a minimum of:<br>Six (6) Cores** |



# 108 Bus System – Core Allocation

| Component | Quantity | # of NovaCor Load Units | Comments |
|---|---|---|---|
| Nodes (1Ø) and controls | (1224-900*) = 324 | 600 units | 2 network solutions/1 subsystem<br>*900 embedded t-line, transformer, and generator nodes not solved by the network solution<br>Generator, breaker, and fault control plus digital input and output signals |
| Single Circuit Lines (3Ø) | 98 | 980 units | Optimized Bergeron model with embedded breakers |
| Double Circuit Lines (2x3Ø) | 7 | 210 units | Optimized Bergeron model with embedded breakers |
| Generator / Transformer (3Ø) | 21 | 420 units | Integrated generator – transformer model (intermediate nodes not counted) |
| Transformer (3Ø) | 17 | 255 units | 3Ø Transformer with Saturation and embedded breakers |
| **Total No.<br>Core Units** | | **2465 units** | **300 units/core x 10 cores/chassis** |
| **Total No.<br>Cores** | | **9<br>Cores** | **One (1) chassis requiring a minimum of:<br>Nine (9) Cores** |